

## 1 Trace

### 1.6.3.5.3 Central Trace Qualifier Unit (TQU\_MCX)

#### Feature Overview

- Dedicated trace enables for the MCX trace units TSU and WTU
- 32 universal 16-bit counters, using programmable combinations of triggers as count and clear signals
- Programmable limit comparator in each counter
- Passing a limit is available as unique trigger for 16 counters
- The counter values of 16 counters can be traced (see WTU\_MCX)
- Pre-scaled reference clock available as trigger tsu\_tc\_trig
- Four triggers from each observation block's TQU
- Four triggers to each observation block's TQU
- Five uncommitted trace enables to each observation block's TQU
- Two TBUF watermark triggers tbuf\_wm\_trg see [Trace bandwidth reduction](#)
- Trigger from OTGS break switch
- Trigger to OTGS break switch
- Trigger to OTGS suspend switch
- Four triggers to package pins (but not on all package variants)
- Four cross-triggers to other MCDS instance
- **Planned for TC49xB-step: countable event pool for performance signals from various sources like PSPR/ DSPR/DLMU, Flash, DMA, SPB**

For the detailed functional description of a central Trace Qualifier Unit see [Chapter 1.5.3.12](#).

#### MCX Trigger pool to Event definition allocation matrix

**Table 133** defines which trigger inputs are available to each Event Definition register (see [Chapter 1.5.3.3](#)) in the corresponding 16-bit wide subset of the trigger pool. Each trigger in the trigger pool is given a row, each Event Definition register (MCXEVTi) occupies one column, and the values in the table represents the index "x" (see [MCX EVT Event Definition Register x](#)) associated with the triggers in each specific Event register.

**Attention:** *The trigger signals tcy\_act[0-3] and tcz\_act[0-3] are not applicable for MCDS2P. Hence they are tied to '1'.*

**Table 133** Trigger Pool to Event Definition Allocation Matrix

Trigger	Trigger [row] assigned to given bit number in MCXEVT[header]															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
break_in											0	0	0	0	0	0
tbuf_wm_trg[0]													1	1		
tbuf_wm_trg[1]															1	1
tsu_tc_trig									0	0			2	2	2	2
tcx_act[0]	0	0	0	0			0	0							3	3
tcx_act[1]	1	1	1	1			1	1	1	1						
tcx_act[2]	2	2			0	0			2	2	1	1				
tcx_act[3]	3	3			1	1					2	2				
tcy_act[0]	4	4	2	2					3	3	3	3				
tcy_act[1]	5	5	3	3	2	2							3	3		

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Table 133 Trigger Pool to Event Definition Allocation Matrix (continued)

Trigger	Trigger [row] assigned to given bit number in MCXEVT[header]															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
tcy_act[2]			4	4			2	2					4	4	4	4
tcy_act[3]			5	5	3	3	3	3							5	5
tcz_act[0]	6	6			4	4			4	4	4	4				
tcz_act[1]	7	7			5	5					5	5	5	5		
tcz_act[2]			6	6	6	6	4	4					6	6		
tcz_act[3]			7	7	7	7	5	5							6	6
spb_act[0]	8	8	8	8					5	5	6	6				
spb_act[1]	9	9	9	9									7	7	7	7
spb_act[2]					8	8	6	6								
spb_act[3]					9	9	7	7								
tcw_act[0]	10	10			10	10							8	8	8	8
tcw_act[1]	11	11			11	11			6	6	7	7				
tcw_act[2]			10	10			8	8	7	7	8	8				
tcw_act[3]			11	11			9	9								
crosstrig[0]	12	12			12	12					9	9	9	9		
crosstrig[1]	13	13			13	13			8	8					9	9
crosstrig[2]			12	12			10	10	9	9						
crosstrig[3]			13	13			11	11								
cnt_trig[0]	14	14	14	14			12	12	10	10						
cnt_trig[1]	15	15	15	15			13	13	11	11						
cnt_trig[2]					14	14	14	14	12	12	10	10	10	10		
cnt_trig[3]					15	15	15	15	13	13	11	11	11	11		
cnt_trig[4]									14	14	12	12	12	12		
cnt_trig[5]									15	15	13	13	13	13		
cnt_trig[6]											14	14	14	14	10	10
cnt_trig[7]											15	15	15	15	11	11
cnt_trig[8]															12	12
cnt_trig[9]															13	13
cnt_trig[10]															14	14
cnt_trig[11]															15	15
cnt_trig[12]																
cnt_trig[13]																
cnt_trig[14]																
cnt_trig[15]																

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Table 134 Trigger Pool to Event Definition Allocation Matrix (continued)

Trigger	Trigger [row] assigned to given bit number in MCXEVT[header]															
	16	17	18	19	20	21	22	23								
break_in	0	0														
tbuf_wm_trg[0]	1	1	0	0												
tbuf_wm_trg[1]					0	0	0	0								
tsu_tc_trig	2	2	1	1	1	1	1	1								
tcx_act[0]	3	3														
tcx_act[1]	4	4	2	2												
tcx_act[2]																
tcx_act[3]																
tcy_act[0]																
tcy_act[1]			3	3												
tcy_act[2]																
tcy_act[3]	5	5														
tcz_act[0]	6	6	4	4												
tcz_act[1]			5	5	2	2										
tcz_act[2]							2	2								
tcz_act[3]																
spb_act[0]																
spb_act[1]																
spb_act[2]	7	7	6	6												
spb_act[3]					3	3										
tcw_act[0]																
tcw_act[1]																
tcw_act[2]																
tcw_act[3]	8	8	7	7												
crosstrig[0]																
crosstrig[1]																
crosstrig[2]							3	3								
crosstrig[3]	9	9														
cnt_trig[0]	10	10														
cnt_trig[1]	11	11														
cnt_trig[2]																
cnt_trig[3]																
cnt_trig[4]					4	4	4	4								
cnt_trig[5]					5	5	5	5								
cnt_trig[6]					6	6	6	6								

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**Table 134 Trigger Pool to Event Definition Allocation Matrix (continued) (continued)**

Trigger	Trigger [row] assigned to given bit number in MCXEVT[header]															
	16	17	18	19	20	21	22	23								
cnt_trig[7]					7	7	7	7								
cnt_trig[8]	12	12	8	8	8	8	8	8								
cnt_trig[9]	13	13	9	9	9	9	9	9								
cnt_trig[10]	14	14	10	10	10	10	10	10								
cnt_trig[11]	15	15	11	11	11	11	11	11								
cnt_trig[12]			12	12	12	12	12	12								
cnt_trig[13]			13	13	13	13	13	13								
cnt_trig[14]			14	14	14	14	14	14								
cnt_trig[15]			15	15	15	15	15	15								

The Event Pool for the Action Definitions (see [Chapter 1.5.3.6](#)) of the MCX is defined in [Table 135](#):

**Table 135 Event Pool Encoding for Action Definitions**

Event ID	Source	Comment
0 ... 23	MCXEVT0 ... MCXEVT23	Events calculated locally in MCX
24 ... 31	sync_rq	Pulsed high for one clock cycle at the beginning of a new paragraph of buffer memory

**MCX Action definition assignment**

The purpose of the Action Definitions is listed in [Table 136](#):

**Table 136 Action Definition Assignment**

Register	Purpose	Function
MCXACT0	tsu_rel_en	TSU emulation clock time stamp enable
MCXACT1	tsu_rel_sync	TSU emulation clock sync message request
MCXACT2	tsu_abs_en	TSU reference clock time stamp enable
MCXACT3	tsu_abs_sync	TSU reference clock sync message request
MCXACT4	wtu_enable[0]	WTU_MCX watch-point message request ID 0
MCXACT5	wtu_enable[1]	WTU_MCX watch-point message request ID 1
MCXACT6	wtu_enable[2]	WTU_MCX watch-point message request ID 2
MCXACT7	wtu_enable[3]	WTU_MCX watch-point message request ID 3
MCXACT8	wtu_enable[4]	WTU_MCX watch-point message request ID 4
MCXACT9	wtu_enable[5]	WTU_MCX watch-point message request ID 5
MCXACT10	wtu_enable[6]	WTU_MCX watch-point message request ID 6
MCXACT11	wtu_enable[7]	WTU_MCX watch-point message request ID 7
MCXACT12	wtu_cnt[0]	WTU_MCX counter message request (MCXCNT0)
MCXACT13	wtu_cnt[1]	WTU_MCX counter message request (MCXCNT1)