

Multi-Core Debug Solution (MCDS)

Table 90 Available signals from TriCore OCDS logic (cont'd)

Name	Source	Description
core_trig6	TR6ADR	Asserted when the IP (TR6EVT.TYP=1) or the R/W address (TR6EVT.TYP=0) match the current value of TR6ADR.
core_trig7	TR7ADR	Asserted when the IP (TR7EVT.TYP=1) or the R/W address (TR7EVT.TYP=0) match the current value of TR7ADR.

1) Note that for an address range trigger only TR0EVT can be used. TR1EVT is then blocked,

Note: Most core triggers are aligned. It is possible to create events based on a certain instruction (indicated by ptu_trig) reading a certain address (core_trig* programmed to match data address). It is however not recommended to use core_trig* for trace qualification when the associated OCDS comparator is programmed for matching the instruction pointer.*

For the detailed functional description of a local Trace Qualifier Unit see [Chapter 8.3.14](#).

Table 179 defines which trigger inputs are available to each Event Definition register (see [Chapter 8.3.4](#)) in the corresponding 16 bit wide subset of the trigger pool. Each trigger in the trigger pool is given a row, each Event Definition register (TCEVTi) occupies one column, and the values in the table represents the index “x” (see [Page 32](#)) associated with the triggers in each specific Event register.

Table 91 Trigger Pool to Event Definition Allocation Matrix

Trigger	Trigger [row] assigned to given bit number in TCEVT[header]															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
core_crevt	0	0	0	0												
core_trig0	1				0				0							
core_trig1		1			1				1							
core_trig2			1			0				0						
core_trig3				1		1				1						
core_trig4					2		0				0					
core_trig5					3		1				1					
core_trig6								0				0				
core_trig7								1				1				
core_tr0evt	2	2					2	2					0		0	
core_tr1evt			2	2		2							1		1	
core_exevt	3		3			3	3							0		0
core_swevt		3		3				3						1		1
core_ea_fine											2	2	2	2	2	2
ptu_trig[0]	4	4							2	2	3	3			3	3
ptu_trig[1]	5	5	4	4					3	3	4	4			4	4
ptu_trig[2]	6	6	5	5	4	4			4	4						
ptu_trig[3]			6	6	5	5										
ptu_trig[4]					6	6	4	4					3	3		
ptu_trig[5]							5	5					4	4		
otu_trig[0]									5	5	5	5				

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Trigger	Trigger [row] assigned to given bit number in TCEVT[header]															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
otu_trig[1]									6	6						
otu_trig[2]											6	6				
dtu_ea_trig[0]	7	7					6						5		5	
dtu_ea_trig[1]	8	8					7						6		6	
dtu_ea_trig[2]			7	7			8						7		7	
dtu_ea_trig[3]			8	8				6							8	
dtu_ea_trig[4]					7	7		7						5		5
dtu_ea_trig[5]					8	8		8						6		6
dtu_ea_trig[6]									7	7	7	7		7		7
dtu_ea_trig[7]									8	8	8	8				8
dtu_dat_trig[0]	9				9				9				8	8	9	9
dtu_dat_trig[1]		9				9				9			9	9	10	10
dtu_dat_trig[2]			9				9				9					
dtu_dat_trig[3]				9				9				9				
dtu_acc_trig[0]	10	10	10	10	10	10	10	10	10	10	10	10	10	10	11	11
dtu_acc_trig[1]					11	11			11	11			11	11	12	12
dtu_acc_trig[2]							11	11			11	11	12	12		
dtu_acc_trig[3]							12	12	12	12					13	13
dcu_sus					12	12			13	13						
dcu_idle							13	13					13	13		
dcu_halt			11	11							12	12				
dcu_isr	11	11			13	13					13	13				
tc_trig[0] STDSW	12	12	12	12	14	14	14	14	14	14	14	14				
tc_trig[1]	13	13	13	13	15	15	15	15	15	15	15	15				
tc_trig[2]	14	14	14	14									14	14	14	14
tc_trig[3]	15	15	15	15									15	15	15	15

The Event Pool for the Action Definitions (see [Chapter 8.3.7](#)) of the POB_TC is defined in [Table 180](#):

Table 92 Event Pool Encoding

Event ID	Source	Comment
0 ... 15	TCEVT0 ... TCEVT15	Events calculated locally in POB_TC
16 ... 19	tc_trig[0] ... tc_trig[3]	Trigger signals from TQU_MCX to TQU_TC