

3.3 Address Map of the On Chip Bus System

This chapter describes the system address map as it is seen from the SRI and SPB bus masters (bus master agents are described in the chapter On Chip Bus System).

All bus master agents can address identical peripherals and memories at identical address. The system address map is visible and valid for all CPUs which means that all peripherals and resources are accessible from all TriCore CPUs and other on chip bus master agents.

Parallel access by more than one bus master agents to one slave agent are executed sequentially. Additionally the SRI and SPB bus do support atomic Read Modify Write sequences from the CPUs. Hardware semaphores for temporary exclusive bus access from one master to a slave are not implemented

3.3.1 Segments 0 to 14

Table 3-2 shows the address map of segments 0 to 14.

Table 3-2 On Chip Bus Address Map of Segment 0 to 14

Seg- ment	Address Range	Size	Description	Access Type	
				Read ¹⁾	Write ²⁾
0-5	0000 0000 _H - 0000 0007 _H	8 byte	Reserved (virtual address space)	SRIBE	SRIBE
	0000 0008 _H - 5FFF FFFF _H	-		SRIBE	SRIBE
6	6000 0000 _H - 6001 DFFF _H	120 Kbyte	CPU1 Data Scratch-Pad SRAM (CPU1.DSPR)	access	access
	6001 E000 _H - 6001 FFFF _H	8 Kbyte	CPU1.Data Cache SRAM (CPU1.DCACHE)	access ³⁾ / SRIBE	access ³⁾ / SRIBE
	6002 0000 _H - 600B FFFF _H	-	Reserved	SRIBE	SRIBE
	600C 0000 _H - 600C 0BFF _H	-	CPU1 Data Cache TAG SRAM ⁴⁾ (CPU1.DTAG)	access ³⁾ / SRIBE	access ³⁾ / SRIBE
	600C 0C00 _H - 600F FFFF _H	-	Reserved	SRIBE	SRIBE
	6010 0000 _H - 6010 7FFF _H	32 Kbyte	CPU1 Program Scratch- Pad SRAM (CPU1.PSPR)	access	access
	6010 8000 _H - 6010 BFFF _H	16 Kbyte	CPU1.Program Cache SRAM (CPU1.PCache)	access ³⁾ / SRIBE	access ³⁾ / SRIBE

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Table 3-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Seg- ment	Address Range	Size	Description	Access Type	
				Read ¹⁾	Write ²⁾
	6010 C000 _H - 601B FFFF _H	-	Reserved	SRIBE	SRIBE
	601C 0000 _H - 601C 17FF _H	-	CPU1 Program Cache TAG SRAM ⁴⁾ (CPU1.PTAG)	access ³⁾ / SRIBE	access ³⁾ / SRIBE
	601C 1800 _H - 6FFF FFFF _H	-	Reserved	SRIBE	SRIBE
7	7000 0000 _H - 7001 1FFF _H	72 Kbyte	CPU0 Data Scratch-Pad SRAM (CPU0.DSPR)	access	access
	7001 2000 _H - 700F FFFF _H	-	Reserved	SRIBE	SRIBE
	7010 0000 _H - 7010 3FFF _H	16 Kbyte	CPU0 Program Scratch- Pad SRAM (CPU0.PSPR)	access	access
	7010 4000 _H - 7010 5FFF _H	8 Kbyte	CPU0.Program Cache SRAM (CPU0.PCache)	access ³⁾ / SRIBE	access ³⁾ / SRIBE
	7010 6000 _H - 701B FFFF _H	-	Reserved	SRIBE	SRIBE
	701C 0000 _H - 701C 0BFF _H	-	CPU0 Program Cache TAG SRAM ⁴⁾ (CPU0.PTAG)	access ³⁾ / SRIBE	access ³⁾ / SRIBE
	701C 0C00 _H - 7FFF FFFF _H	-	Reserved	SRIBE	SRIBE
8	8000 0000 _H - 800F FFFF _H	1 Mbyte	Program Flash 0 (PF0)	access	access ²⁾
	8010 0000 _H - 8027 FFFF _H	1.5 Mbyte	Program Flash 1 (PF1)	access	access ²⁾
	8028 0000 _H - 8FE6 FFFF _H	-	Reserved	SRIBE	SRIBE
	8FE7 0000 _H - 8FE7 7FFF _H	32 Kbyte	Online Data Acquisition (OLD A)	SRIBE	access ⁵⁾ / SRIBE
	8FE7 8000 _H - 8FFF 7FFF _H	-	Reserved	SRIBE	SRIBE

Memory Maps
Table 3-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Seg- ment	Address Range	Size	Description	Access Type	
				Read ¹⁾	Write ²⁾
9	8FFF 8000 _H - 8FFF FFFF _H	32 Kbyte	Boot ROM (BROM)	access	SRIBE
	9000 0000 _H - 9EFF FFFF _H	-	Reserved	SRIBE	SRIBE
	9F00 0000 _H - 9F07 FFFF _H	512 Kbyte	Reserved for TC26x B- Step Emulation Device Memory (EMEM)	SRIBE	SRIBE ⁶⁾
	9F08 0000 _H - 9F0F FFFF _H	-	Reserved	SRIBE	SRIBE
	9F10 0000 _H - 9F10 3FFF _H	16 Kbyte	Reserved for TC26x B- Step Emulation Device Memory (EMEM)	SRIBE	SRIBE ⁶⁾
	9F10 4000 _H - 9FFF FFFF _H	-	Reserved	SRIBE	SRIBE
10	A000 0000 _H - A00F FFFF _H	1 Mbyte	Program Flash 0 (PF0)	access	access ²⁾
	A010 0000 _H - A027 FFFF	1.5 Mbyte	Program Flash 1 (PF1)	access	access ²⁾
	A028 0000 _H - AEFF FFFF _H	-	Reserved	SRIBE	SRIBE
	AF00 0000 _H - AF0F FFFF _H	1 Mbyte	Data Flash 0 (DF0 Address Range)	access	access ²⁾⁷⁾
	AF10 0000 _H - AF10 3FFF _H	16 Kbyte	Data Flash 0 (DF0 Address Range)	access	access ²⁾⁷⁾
	AF10 4000 _H - AFE6 FFFF _H	-	Reserved	SRIBE	SRIBE
	AFE7 0000 _H - AFE7 7FFF _H	32 Kbyte	Online Data Acquisition (OLDA)	SRIBE	access ⁵⁾ / SRIBE
	AFE7 8000 _H - AFF7 7FFF _H	-	Reserved	SRIBE	SRIBE
	AFFF 8000 _H - AFFF FFFF _H	32 Kbyte	Boot ROM (BROM)	access	SRIBE
11	B000 0000 _H - BDFF FFFF _H	-	Reserved	SRIBE	SRIBE

Memory Maps
Table 3-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Seg- ment	Address Range	Size	Description	Access Type	
				Read ¹⁾	Write ²⁾
	BE00 0000 _H - BE07 FFFF _H	512 Kbyte	Reserved for FFT Accelerator (ADAS Device only)	SRIBE	SRIBE ⁶⁾
	BE08 0000 _H - BE0F FFFF _H	-	Reserved	SRIBE	SRIBE
	BE10 0000 _H - BE17 FFFF _H	512 Kbyte	Reserved for FFT Accelerator (ADAS Device only)	SRIBE	SRIBE ⁶⁾
	BE18 0000 _H - BEFF FFFF _H	-	Reserved	SRIBE	SRIBE
	BF00 0000 _H - BF07 FFFF _H	512 Kbyte	Reserved for TC26x B- Step Emulation Device Memory (EMEM)	SRIBE	SRIBE ⁶⁾
	BF08 0000 _H - BF0F FFFF _H	-	Reserved	SRIBE	SRIBE
	BF10 0000 _H - BF10 3FFF _H	16 Kbyte	Reserved for TC26x B- Step Emulation Device Memory (EMEM)	SRIBE	SRIBE ⁶⁾
	BF10 4000 _H - BFFF FFFF _H	-	Reserved	SRIBE	SRIBE
12	C000 0000 _H - CFFF FFFF _H	-	Reserved ⁸⁾	SRIBE	SRIBE
13	D000 0000 _H - DFFF FFFF _H	-	Reserved ⁸⁾	SRIBE	SRIBE
14	E000 0000 _H - EFFF FFFF _H	-	Reserved	SRIBE	SRIBE
15	F000 0000 _H - FFFF FFFF _H	256 Mbyte	see Table 3-3		

1) A read transaction through the SRI to FPI bridge that is terminated with Bus Error will result in Bus Errors on SRI and FPI (valid for transactions from FPI to SRI and SRI to FPI).

2) Write access to Flash resources are handled by the PMU module (Flash command sequence, see PMU chapter for details).

3) PCache/DCache SRAMs (and the corresponding TAG SRAMs) can be only accessed when mapped into the address space (PCache / DCache disabled. See MTU chapter, register MTU_MEMMAP for details).

Memory Maps

- 4) TAG SRAMs are not meant to be used as general SRAMs and can be accessed only with single data access and only with 64 bit aligned address. Mapping of TAG SRAMs in the address map can be used as additional option for memory testing.
- 5) Online Data Acquisition address space can be disabled/enabled via LMU control register bit LMU_MEMCON.OLDAEN. TC1.6P access to OLDA address space via segment 8 (cached) results in SRIBE independent of the LMU_MEMCON.OLDAEN bit setting.
- 6) This address range is mapped to the LMU module. A read/write from/to this address range will result in an SRI Bus Error initiated by the LMU module,
- 7) DF0 is the address where all Data Flash blocks are mapped to. The details about the Data Flash block sizes, segmentation and exact mapping are described in the chapter PMU.
- 8) See also chapter 'CPU, 'Local and Global Addressing' for CPU local views to segment 'C' and segment 'D'.

3.3.2 Segment 15

Table 3-3 shows the address map of segment 'F' as seen from the SRI and SPB bus masters (bus master agents are described in the chapter On Chip Bus System).

Table 3-1 gives an overview about the address mapping of the module address ranges:

- which modules are mapped into the first 16 KB of segment 'F' and can be accessed by the TC1.6E/P with absolute addressing modes (left side)
- examples of covering modules with relative addressing mode (base address +/- 32 KB, in the middle)

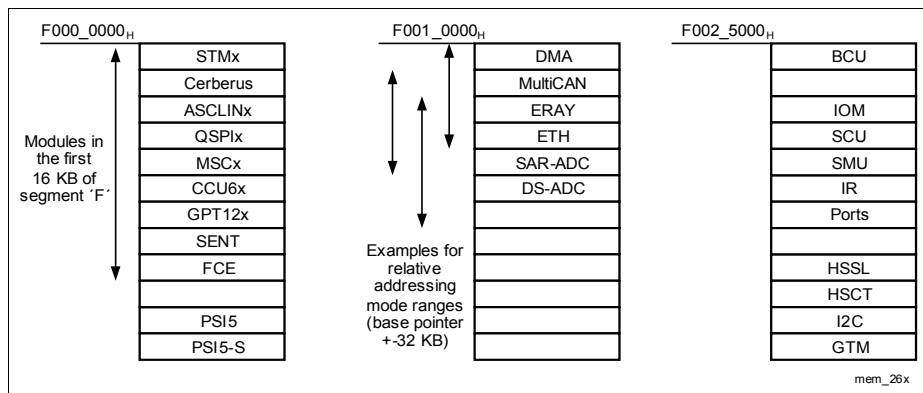


Figure 3-1 Segment F Structure

Please note that **Table 3-3** describes the mapping of modules to segment F. The details of the module address ranges can be found in the module chapters register overview.

Table 3-3 On Chip Bus Address Map of Segment 15

Unit	Address Range	Size	Access Type	
			Read	Write
System Timer 0 (STM0)	F000 0000 _H - F000 00FF _H	256 byte	access	access
System Timer 1 (STM1)	F000 0100 _H - F000 01FF _H	256 byte	access	access
Reserved	F000 0200 _H - F000 03FF _H	—	SPBBE	SPBBE
On-Chip Debug Support (Cerberus)	F000 0400 _H - F000 05FF _H	2x256 byte	access	access

Memory Maps
Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
ASCLIN0 (ASCLIN0)	F000 0600 _H - F000 06FF _H	256 byte	access	access
ASCLIN1 (ASCLIN1)	F000 0700 _H - F000 07FF _H	256 byte	access	access
ASCLIN2 (ASCLIN2)	F000 0800 _H - F000 08FF _H	256 byte	access	access
ASCLIN3 (ASCLIN3)	F000 0900 _H - F000 09FF _H	256 byte	access	access
Reserved	F000 0A00 _H - F000 1BFF _H	–	SPBBE	SPBBE
QUEUED SPI 0 (QSPI0)	F000 1C00 _H - F000 1CFF _H	256 byte	access	access
QUEUED SPI 1 (QSPI1)	F000 1D00 _H - F000 1DFF _H	256 byte	access	access
QUEUED SPI 2 (QSPI2)	F000 1E00 _H - F000 1EFF _H	256 byte	access	access
QUEUED SPI 3 (QSPI3)	F000 1F00 _H - F000 1FFF _H	256 byte	access	access
Reserved	F000 2000 _H - F000 25FF _H	–	SPBBE	SPBBE
MicroSecond Bus Controller 0 (MSC0)	F000 2600 _H - F000 26FF _H	256 byte	access	access
MicroSecond Bus Controller 1 (MSC1)	F000 2700 _H - F000 27FF _H	256 byte	access	access
Reserved	F000 2800 _H - F000 29FF _H	–	SPBBE	SPBBE
Capture/Compare Unit 6 0 (CCU60)	F000 2A00 _H - F000 2AFF _H	256 byte	access	access
Capture/Compare Unit 6 1 (CCU61)	F000 2B00 _H - F000 2BFF _H	256 byte	access	access
Reserved	F000 2C00 _H - F000 2DFF _H	–	SPBBE	SPBBE

Memory Maps
Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
General Purpose Timer 12 0 (GPT120)	F000 2E00 _H - F000 2EFF _H	256 byte	access	access
Reserved	F000 2F00 _H - F000 2FFF _H	–	SPBBE	SPBBE
SENT Module (SENT)	F000 3000 _H - F000 3AFF _H	11x256 byte	access	access
Reserved	F000 3B00 _H - F000 3EFF _H	–	SPBBE	SPBBE
Flexible CRC Engine (FCE)	F000 3F00 _H - F000 3FFF _H	256 byte	access	access
Reserved	F000 4000 _H - F000 4FFF _H	–	SPBBE	SPBBE
PSI5 (PSI5)	F000 5000 _H - F000 6FFF _H	8 KByte	access	access
PSI5-S (PSI5-S)	F000 7000 _H - F000 7FFF _H	4 KByte	access	access
Reserved	F000 8000 _H - F000 FFFF _H	–	SPBBE	SPBBE
Direct Memory Access Controller (DMA)	F001 0000 _H - F001 3FFF _H	16 KByte	access	access
Reserved	F001 4000 _H - F001 7FFF _H	–	SPBBE	SPBBE
MultiCAN Controller (CAN)	F001 8000 _H - F001 BFFF _H	16 Kbyte	access	access
FlexRay™ Protocol Controller (E-Ray)	F001 C000 _H - F001 CFFF _H	4 Kbyte	access	access
Ethernet Controller System Control Register (ETH)	F001 D000 _H - F001 D0FF _H	256 byte	access	access
Reserved	F001 D100 _H - F001 DFFF _H	–	SPBBE	SPBBE
Ethernet Controller (ETH)	F001 E000 _H - F001 FFFF _H	8 KByte	access	access

Memory Maps
Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
Analog-to-Digital Converter (VADC)	F002 0000 _H - F002 3FFF _H	16 KByte	access	access
Delta Sigma Ditigal Analog-to-Digital Converter (DSADC)	F002 4000 _H - F002 4FFF _H	4 Kbyte	access	access
Reserved	F002 5000 _H - F002 FFFF _H	–	SPBBE	SPBBE
System Peripheral Bus Control Unit (BCU)	F003 0000 _H - F003 00FF _H	256 byte	access	access
Reserved	F003 0100 _H - F003 4FFF _H	–	SPBBE	SPBBE
I/O Monitor (IOM)	F003 5000 _H - F003 51FF _H	2x256 byte	access	access
Reserved	F003 5200 _H - F003 5FFF _H	–	SPBBE	SPBBE
System Control Unit (SCU)	F003 6000 _H - F003 63FF _H	1 Kbyte	access	access
Reserved	F003 6400 _H - F003 67FF _H	–	SPBBE	SPBBE
Safety Management Unit (SMU)	F003 6800 _H - F003 6FFF _H	2 Kbyte	access	access
Interrupt Router (IR)	F003 7000 _H - F003 7FFF _H	4 Kbyte	access	access
Interrupt Router (IR) SRC Registers	F003 8000 _H - F003 9FFF _H	8 Kbyte	access	access
Port 00	F003 A000 _H - F003 A0FF _H	256 byte	access	access
Reserved	F003 A100 _H - F003 A1FF _H	256 byte	SPBBE	SPBBE
Port 02	F003 A200 _H - F003 A2FF _H	256 byte	access	access
Reserved	F003 A300 _H - F003 AFFF _H	–	SPBBE	SPBBE

Memory Maps
Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
Port 10	F003 B000 _H - F003 B0FF _H	256 byte	access	access
Port 11	F003 B100 _H - F003 B1FF _H	256 byte	access	access
Reserved	F003 B200 _H - F003 B2FF _H	–	SPBBE	SPBBE
Port 13	F003 B300 _H - F003 B3FF _H	256 byte	access	access
Port 14	F003 B400 _H - F003 B4FF _H	256 byte	access	access
Port 15	F003 B500 _H - F003 B5FF _H	256 byte	access	access
Reserved	F003 B600 _H - F003 BFFF _H	–	SPBBE	SPBBE
Port 20	F003 C000 _H - F003 C0FF _H	256 byte	access	access
Port 21	F003 C100 _H - F003 C1FF _H	256 byte	access	access
Port 22	F003 C200 _H - F003 C2FF _H	256 byte	access	access
Port 23	F003 C300 _H - F003 C3FF _H	256 byte	access	access
Reserved	F003 C400 _H - F003 D1FF _H	–	SPBBE	SPBBE
Port 32	F003 D200 _H - F003 D2FF _H	256 byte	access	access
Port 33	F003 D300 _H - F003 D3FF _H	256 byte	access	access
Reserved	F003 D400 _H - F003 DFFF _H	–	SPBBE	SPBBE
Port 40	F003 E000 _H - F003 E0FF _H	256 byte	access	access

Memory Maps
Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	F003 E100 _H - F005 FFFF _H	–	SPBBE	SPBBE
Memory Test Unit (MTU)	F006 0000 _H - F006 FFFF _H	64 Kbyte	access	access
Reserved	F007 0000 _H - F007 FFFF _H	–	SPBBE	SPBBE
High Speed Serial Link (HSSL)	F008 0000 _H - F008 03FF _H	4x256 byte	access	access
Reserved	F008 0400 _H - F008 FFFF _H	–	SPBBE	SPBBE
High Speed Communication Tunnel (HSCT)	F009 0000 _H - F009 FFFF _H	64 Kbyte	access	access
Reserved	F00A 0000 _H - F00B FFFF _H	–	SPBBE	SPBBE
I2C 0 (I2C0)	F00C 0000 _H - F00C FFFF _H	64 Kbyte	access	access
I2C 0 System Control Register (I2C0)	F00D 0000 _H - F00D 00FF _H	256 byte	access	access
Reserved	F00D 0100 _H - F00F FFFF _H	–	SPBBE	SPBBE
Global Timer Module (GTM)	F010 0000 _H - F019 FFFF _H	640 Kbyte	access	access
Reserved	F01A 0000 _H - F7FF FFFF _H	–	SPBBE	SPBBE
Reserved	F800 0000 _H - F800 04FF _H	–	SRIBE	SRIBE
Program Memory Unit 0 (PMU0)	F800 0500 _H - F800 05FF _H	256 byte	access	access
Reserved	F800 0600 _H - F800 0FFF _H	–	SRIBE	SRIBE
Flash Register (PMU0)	F800 1000 _H - F800 23FF _H	5 Kbyte	access	access

Memory Maps
Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	F800 2400 _H - F86F FFFF _H	–	SRIBE	SRIBE
SRI Crossbar (XBar_SRI)	F870 0000 _H - F870 04FF _H	5x256 byte	access	access
Reserved	F870 0500 _H - F870 07FF _H	–	SRIBE	SRIBE
Local Memory Unit (LMU)	F870 0800 _H - F870 08FF _H	256 byte	access	access
Reserved	F870 0900 _H - F870 0BFF _H	–	SRIBE	SRIBE
FFT Accelerator (FFT, Emulation Device only)	F870 0C00 _H - F870 0CFF _H	256 byte	access	access
Reserved	F870 0D00 _H - F87F FFFF _H	–	SRIBE	SRIBE
CPU0 SFR	F880 0000 _H - F880 FFFF _H	64 KByte	access	access
CPU0 CSFR	F881 0000 _H - F881 FFFF _H	64 KByte	access	access
CPU1 SFR	F882 0000 _H - F882 FFFF _H	64 KByte	access	access
CPU1 CSFR	F883 0000 _H - F883 FFFF _H	64 KByte	access	access
Reserved	F884 0000 _H - F8FF FFFF _H	–	SRIBE	SRIBE
Reserved for TC26x B-Step Emulation Device Registers (ED Reg)	F900 0000 _H - F90F FFFF _H	1 MB	access	access
Reserved	F910 0000 _H - FFFF FFFF _H	–	SRIBE	SRIBE