

### Segment 13

This memory segment is reserved.

### Segment 14

This memory segment is reserved.

### Segment 15

The lower 128 Mbyte is SPB address space and the upper 128 Mbyte is SRI address space.

## 2.5 Address Map of the On Chip Bus System

This chapter describes the system address map as it is seen from the on chip bus masters (bus master agents are described in the chapter On Chip Bus System).

All bus master agents can address identical peripherals and memories at identical address. The system address map is visible and valid for all CPUs which means that all peripherals and resources are accessible from all TriCore CPUs and other on chip bus master agents.

Parallel access by more than one bus master agents to one slave agent are executed sequentially. Additionally the SRI and SPB bus do support atomic Read Modify Write sequences from the CPUs.

### 2.5.1 Segments 0 to 14

**Table 1-4** shows the address map of segments 0 to 14.

#### Notes

1. *Read Access Type: A read transaction through the SRI to FPI bridge that is terminated with Bus Error will result in Bus Errors on SRI and FPI (valid for transactions from FPI to SRI and SRI to FPI).*
2. *Write Access Type: Write access to Flash resources are handled by the PMU module (Flash command sequence, see PMU chapter for details).*

**Table 2-2 On Chip Bus Address Map of Segment 0 to 14**

Segment	Address Range	Size	Description	Access Type	
				Read	Write
0	0000 0000 <sub>H</sub> - 0000 0007 <sub>H</sub>	8 Byte	Reserved (virtual address space)	SRIBE	SRIBE
	0000 0008 <sub>H</sub> - 0FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
1	1000 0000 <sub>H</sub> - 1001 7FFF <sub>H</sub>	96 Kbyte	CPU5 Data Scratch-Pad SRAM (CPU5 DSPR)	Access	Access
	1001 8000 <sub>H</sub> - 1001 BFFF <sub>H</sub>	16 Kbyte	CPU5. Data Cache SRAM (CPU5 DCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	1001 C000 <sub>H</sub> - 100B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	100C 0000 <sub>H</sub> - 100C 17FF <sub>H</sub>	-	CPU5 Data Cache TAG SRAM <sup>2)</sup> (CPU5 DTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	100C 1800 <sub>H</sub> - 100F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	1010 0000 <sub>H</sub> - 1010 FFFF <sub>H</sub>	64 Kbyte	CPU5 Program Scratch-Pad SRAM (CPU5 PSPR)	Access	Access
	1011 0000 <sub>H</sub> - 1011 7FFF <sub>H</sub>	32 Kbyte	CPU5. Program Cache SRAM (CPU5 PCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	1011 8000 <sub>H</sub> - 101B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE

Table 2-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
	101C 0000 <sub>H</sub> - 101C 2FFF <sub>H</sub>	-	CPU5 Program Cache TAG SRAM <sup>2)</sup> (CPU5 PTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	101C 3000 <sub>H</sub> - 1FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
2	2000 0000 <sub>H</sub> - 2FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
3	3000 0000 <sub>H</sub> - 3001 7FFF <sub>H</sub>	96 Kbyte	CPU4 Data Scratch-Pad SRAM (CPU4 DSPR)	Access	Access
	3001 8000 <sub>H</sub> - 3001 BFFF <sub>H</sub>	16 Kbyte	CPU4. Data Cache SRAM (CPU4 DCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	3001 C000 <sub>H</sub> - 300B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	300C 0000 <sub>H</sub> - 300C 17FF <sub>H</sub>	-	CPU4 Data Cache TAG SRAM <sup>2)</sup> (CPU4 DTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	300C 1800 <sub>H</sub> - 300F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	3010 0000 <sub>H</sub> - 3010 FFFF <sub>H</sub>	64 Kbyte	CPU4 Program Scratch-Pad SRAM (CPU4 PSPR)	Access	Access
	3011 0000 <sub>H</sub> - 3011 7FFF <sub>H</sub>	32 Kbyte	CPU4.Program Cache SRAM (CPU4 PCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	3011 8000 <sub>H</sub> - 301B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	301C 0000 <sub>H</sub> - 301C 2FFF <sub>H</sub>	-	CPU4 Program Cache TAG SRAM <sup>2)</sup> (CPU4 PTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	301C 3000 <sub>H</sub> - 3FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	4000 0000 <sub>H</sub> - 4001 7FFF <sub>H</sub>	96 Kbyte	CPU3 Data Scratch-Pad SRAM (CPU3 DSPR)	Access	Access
4	4001 8000 <sub>H</sub> - 4001 BFFF <sub>H</sub>	16 Kbyte	CPU3. Data Cache SRAM (CPU3 DCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	4001 C000 <sub>H</sub> - 400B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	400C 0000 <sub>H</sub> - 400C 17FF <sub>H</sub>	-	CPU3 Data Cache TAG SRAM <sup>2)</sup> (CPU3 DTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	400C 1800 <sub>H</sub> - 400F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	4010 0000 <sub>H</sub> - 4010 FFFF <sub>H</sub>	64 Kbyte	CPU3 Program Scratch-Pad SRAM (CPU3 PSPR)	Access	Access
	4011 0000 <sub>H</sub> - 4011 7FFF <sub>H</sub>	32 Kbyte	CPU3.Program Cache SRAM (CPU3 PCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	4011 8000 <sub>H</sub> - 401B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	401C 0000 <sub>H</sub> - 401C 2FFF <sub>H</sub>	-	CPU3 Program Cache TAG SRAM <sup>2)</sup> (CPU3 PTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	401C 3000 <sub>H</sub> - 4FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	5000 0000 <sub>H</sub> - 5001 7FFF <sub>H</sub>	96 Kbyte	CPU2 Data Scratch-Pad SRAM (CPU2 DSPR)	Access	Access
	5001 8000 <sub>H</sub> - 5001 BFFF <sub>H</sub>	16 Kbyte	CPU2. Data Cache SRAM (CPU2 DCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE

Table 2-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
	5001 C000 <sub>H</sub> - 500B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	500C 0000 <sub>H</sub> - 500C 17FF <sub>H</sub>	-	CPU2 Data Cache TAG SRAM <sup>2)</sup> (CPU2 DTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	500C 1800 <sub>H</sub> - 500F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	5010 0000 <sub>H</sub> - 5010 FFFF <sub>H</sub>	64 Kbyte	CPU2 Program Scratch-Pad SRAM (CPU2 PSPR)	Access	Access
	5011 0000 <sub>H</sub> - 5011 7FFF <sub>H</sub>	32 Kbyte	CPU2.Program Cache SRAM (CPU2 PCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	5011 8000 <sub>H</sub> - 501B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	501C 0000 <sub>H</sub> - 501C 2FFF <sub>H</sub>	-	CPU2 Program Cache TAG SRAM <sup>2)</sup> (CPU2 PTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	501C 3000 <sub>H</sub> - 5FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
6	6000 0000 <sub>H</sub> - 6001 7FFF <sub>H</sub>	96 Kbyte	CPU1 Data Scratch-Pad SRAM (CPU1 DSPR)	Access	Access
	6001 8000 <sub>H</sub> - 6001 BFFF <sub>H</sub>	16 Kbyte	CPU1. Data Cache SRAM (CPU1 DCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	6001 C000 <sub>H</sub> - 600B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	600C 0000 <sub>H</sub> - 600C 17FF <sub>H</sub>	-	CPU1 Data Cache TAG SRAM <sup>2)</sup> (CPU1 DTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	600C 1800 <sub>H</sub> - 600F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	6010 0000 <sub>H</sub> - 6010 FFFF <sub>H</sub>	64 Kbyte	CPU1 Program Scratch-Pad SRAM (CPU1 PSPR)	Access	Access
	6011 0000 <sub>H</sub> - 6011 7FFF <sub>H</sub>	32 Kbyte	CPU1.Program Cache SRAM (CPU1 PCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	6011 8000 <sub>H</sub> - 601B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	601C 0000 <sub>H</sub> - 601C 2FFF <sub>H</sub>	-	CPU1 Program Cache TAG SRAM <sup>2)</sup> (CPU1 PTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	601C 3000 <sub>H</sub> - 6FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
7	7000 0000 <sub>H</sub> - 7001 7FFF <sub>H</sub>	96 Kbyte	CPU0 Data Scratch-Pad SRAM (CPU0 DSPR)	Access	Access
	7001 8000 <sub>H</sub> - 7001 BFFF <sub>H</sub>	16 Kbyte	CPU0. Data Cache SRAM (CPU0 DCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	7001 C000 <sub>H</sub> - 700B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	700C 0000 <sub>H</sub> - 700C 17FF <sub>H</sub>	-	CPU0 Data Cache TAG SRAM <sup>2)</sup> (CPU0 DTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	700C 1800 <sub>H</sub> - 700F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	7010 0000 <sub>H</sub> - 7010 FFFF <sub>H</sub>	64 Kbyte	CPU0 Program Scratch-Pad SRAM (CPU0 PSPR)	Access	Access
	7011 0000 <sub>H</sub> - 7011 7FFF <sub>H</sub>	32 Kbyte	CPU0.Program Cache SRAM (CPU0 PCACHE)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE

Table 2-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
	7011 8000 <sub>H</sub> - 701B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	701C 0000 <sub>H</sub> - 701C 2FFF <sub>H</sub>	-	CPU0 Program Cache TAG SRAM <sup>2)</sup> (CPU0 PTAG)	Access <sup>1)</sup> / SRIBE	Access <sup>1)</sup> / SRIBE
	701C 3000 <sub>H</sub> - 7FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
8	8000 0000 <sub>H</sub> - 802F FFFF <sub>H</sub>	3 Mbyte	Program Flash 0 (PF0)	Access	SRIBE
	8030 0000 <sub>H</sub> - 805F FFFF <sub>H</sub>	3 Mbyte	Program Flash 1 (PF1)	Access	SRIBE
	8060 0000 <sub>H</sub> - 808F FFFF <sub>H</sub>	3 Mbyte	Program Flash 2 (PF2)	Access	SRIBE
	8090 0000 <sub>H</sub> - 80BF FFFF <sub>H</sub>	3 Mbyte	Program Flash 3 (PF3)	Access	SRIBE
	80C0 0000 <sub>H</sub> - 80EF FFFF <sub>H</sub>	3 Mbyte	Program Flash 4 (PF4)	Access	SRIBE
	80F0 0000 <sub>H</sub> - 80FF FFFF <sub>H</sub>	1 Mbyte	Program Flash 5 (PF5)	Access	SRIBE
	8100 0000 <sub>H</sub> - 87FF FFFF <sub>H</sub>	112 Mbyte	External EBU Space	Access	Access
	8800 0000 <sub>H</sub> - 8800 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 0 (EC0)	Access	SRIBE
	8800 4000 <sub>H</sub> - 882F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	8830 0000 <sub>H</sub> - 8830 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 1 (EC1)	Access	SRIBE
	8830 4000 <sub>H</sub> - 885F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	8860 0000 <sub>H</sub> - 8860 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 2 (EC2)	Access	SRIBE
	8860 4000 <sub>H</sub> - 888F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	8890 0000 <sub>H</sub> - 8890 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 3 (EC3)	Access	SRIBE
	8890 4000 <sub>H</sub> - 88BF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	88C0 0000 <sub>H</sub> - 88C0 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 4 (EC4)	Access	SRIBE
	88C0 4000 <sub>H</sub> - 88EF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	88F0 0000 <sub>H</sub> - 88F0 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 5 (EC5)	Access	SRIBE
	88F0 4000 <sub>H</sub> - 8FE6 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	8FE7 0000 <sub>H</sub> - 8FE7 FFFF <sub>H</sub>	64 Kbyte	Online Data Acquisition (OLDA)	SRIBE	Access / SRIBE
	8FE8 0000 <sub>H</sub> - 8FFF 7FFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	8FFF 8000 <sub>H</sub> - 8FFF FFFF <sub>H</sub>	32 Kbyte	Boot ROM (BROM)	Access	SRIBE
9	9000 0000 <sub>H</sub> - 9000 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU0 DLMU)	Access	Access
	9001 0000 <sub>H</sub> - 9001 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU1 DLMU)	Access	Access
	9002 0000 <sub>H</sub> - 9002 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU2 DLMU)	Access	Access
	9003 0000 <sub>H</sub> - 9003 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU3 DLMU)	Access	Access
	9004 0000 <sub>H</sub> - 9007 FFFF <sub>H</sub>	256 Kbyte	LMU (LMU0 LMURAM)	Access	Access
	9008 0000 <sub>H</sub> - 900B FFFF <sub>H</sub>	256 Kbyte	LMU (LMU1 LMURAM)	Access	Access
	900C 0000 <sub>H</sub> - 900F FFFF <sub>H</sub>	256 Kbyte	LMU (LMU2 LMURAM)	Access	Access
	9010 0000 <sub>H</sub> - 9013 FFFF <sub>H</sub>	256 Kbyte	LMU (LMU3 LMURAM)	Access	Access
	9014 0000 <sub>H</sub> - 9014 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU4 DLMU)	Access	Access
	9015 0000 <sub>H</sub> - 9015 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU5 DLMU)	Access	Access
	9016 0000 <sub>H</sub> - 903F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE

Table 2-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
	9040 0000 <sub>H</sub> - 9040 7FFF <sub>H</sub>	32 Kbyte	DAM (DAM0 RAM0)	Access	Access
	9040 8000 <sub>H</sub> - 9040 FFFF <sub>H</sub>	32 Kbyte	DAM (DAM0 RAM1)	Access	Access
	9041 0000 <sub>H</sub> - 9041 7FFF <sub>H</sub>	32 Kbyte	DAM (DAM1 RAM0)	Access	Access
	9041 8000 <sub>H</sub> - 9041 FFFF <sub>H</sub>	32 Kbyte	DAM (DAM1 RAM1)	Access	Access
	9042 0000 <sub>H</sub> - 97FF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	9800 0000 <sub>H</sub> - 9800 1FFF <sub>H</sub>	8 Kbyte	MINIMCDS Trace SRAM (TRAM)	Access	Access
	9800 2000 <sub>H</sub> - 98FF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	9900 0000 <sub>H</sub> - 990F FFFF <sub>H</sub>	1 Mbyte	Extension Memory 0 (EMEM0)	Access <sup>3)</sup>	Access <sup>3)</sup>
	9910 0000 <sub>H</sub> - 991F FFFF <sub>H</sub>	1 Mbyte	Extension Memory 1 (EMEM1)	Access <sup>3)</sup>	Access <sup>3)</sup>
	9920 0000 <sub>H</sub> - 992F FFFF <sub>H</sub>	1 Mbyte	Extension Memory 2 (EMEM2)	Access <sup>3)</sup>	Access <sup>3)</sup>
	9930 0000 <sub>H</sub> - 993F FFFF <sub>H</sub>	1 Mbyte	Extension Memory 3 (EMEM3)	Access <sup>3)</sup>	Access <sup>3)</sup>
	9940 0000 <sub>H</sub> - 9947 FFFF <sub>H</sub>	512 Kbyte	Extra Trace Memory (XTM) (only 16 Kbyte physical SRAM)	Access	Access
	9948 0000 <sub>H</sub> - 9FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
10	A000 0000 <sub>H</sub> - A02F FFFF <sub>H</sub>	3 Mbyte	Program Flash 0 (PF0)	Access	SRIBE
	A030 0000 <sub>H</sub> - A05F FFFF <sub>H</sub>	3 Mbyte	Program Flash 1 (PF1)	Access	SRIBE
	A060 0000 <sub>H</sub> - A08F FFFF <sub>H</sub>	3 Mbyte	Program Flash 2 (PF2)	Access	SRIBE
	A090 0000 <sub>H</sub> - A0BF FFFF <sub>H</sub>	3 Mbyte	Program Flash 3 (PF3)	Access	SRIBE
	A0C0 0000 <sub>H</sub> - A0EF FFFF <sub>H</sub>	3 Mbyte	Program Flash 4 (PF4)	Access	SRIBE
	A0F0 0000 <sub>H</sub> - A0FF FFFF <sub>H</sub>	1 Mbyte	Program Flash 5 (PF5)	Access	SRIBE
	A100 0000 <sub>H</sub> - A7FF FFFF <sub>H</sub>	112 Mbyte	External EBU Space	Access	Access
	A800 0000 <sub>H</sub> - A800 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 0 (EC0)	Access	SRIBE
	A800 4000 <sub>H</sub> - A807 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A808 0000 <sub>H</sub> - A80B FFFF <sub>H</sub>	256 Kbyte	PFI User Registers 0 (PFI0)	Access	SRIBE
	A80C 0000 <sub>H</sub> - A82F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A830 0000 <sub>H</sub> - A830 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 1 (EC1)	Access	SRIBE
	A830 4000 <sub>H</sub> - A837 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A838 0000 <sub>H</sub> - A83B FFFF <sub>H</sub>	256 Kbyte	PFI User Registers 1 (PFI1)	Access	SRIBE
	A83C 0000 <sub>H</sub> - A85F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A860 0000 <sub>H</sub> - A860 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 2 (EC2)	Access	SRIBE
	A860 4000 <sub>H</sub> - A867 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A868 0000 <sub>H</sub> - A86B FFFF <sub>H</sub>	256 Kbyte	PFI User Registers 2 (PFI2)	Access	SRIBE
	A86C 0000 <sub>H</sub> - A88F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A890 0000 <sub>H</sub> - A890 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 3 (EC3)	Access	SRIBE
	A890 4000 <sub>H</sub> - A897 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A898 0000 <sub>H</sub> - A89B FFFF <sub>H</sub>	256 Kbyte	PFI User Registers 3 (PFI3)	Access	SRIBE
	A89C 0000 <sub>H</sub> - A8BF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A8C0 0000 <sub>H</sub> - A8C0 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 4 (EC4)	Access	SRIBE

Table 2-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
	A8C0 4000 <sub>H</sub> - A8C7 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A8C8 0000 <sub>H</sub> - A8CB FFFF <sub>H</sub>	256 Kbyte	PFI User Registers 4 (PFI4)	Access	SRIBE
	A8CC 0000 <sub>H</sub> - A8EF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A8F0 0000 <sub>H</sub> - A8F0 3FFF <sub>H</sub>	16 Kbyte	Erase Counter 5 (EC5)	Access	SRIBE
	A8F0 4000 <sub>H</sub> - A8F7 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	A8F8 0000 <sub>H</sub> - A8FB FFFF <sub>H</sub>	256 Kbyte	PFI User Registers 5 (PFI5)	Access	SRIBE
	A8FC 0000 <sub>H</sub> - AEFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AF00 0000 <sub>H</sub> - AF0F FFFF <sub>H</sub>	1 Mbyte	Data Flash 0 EEPROM (DF0) Host Comd. Sequence Interpreter	Access	Access <sup>4)</sup>
	AF10 0000 <sub>H</sub> - AF3F FFFF <sub>H</sub>	3 Mbyte	Reserved	SRIBE	SRIBE
	AF40 0000 <sub>H</sub> - AF40 5FFF <sub>H</sub>	24 Kbyte	Data Flash 0 UCB (DF0)	Access	SRIBE
	AF40 6000 <sub>H</sub> - AF7F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AF80 0000 <sub>H</sub> - AF80 FFFF <sub>H</sub>	64 Kbyte	Data Flash 0 CFS (DF0)	Access	SRIBE
	AF81 0000 <sub>H</sub> - AFBF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AFC0 0000 <sub>H</sub> - AFC1 FFFF <sub>H</sub>	128 Kbyte	Data Flash 1 EEPROM (DF1) HSM Comd. Sequence Interpreter	Access	Access <sup>5)</sup>
	AFC2 0000 <sub>H</sub> - AFC3 FFFF <sub>H</sub>	128 Kbyte	Reserved	SRIBE	SRIBE
	AFC4 0000 <sub>H</sub> - AFE6 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AFE7 0000 <sub>H</sub> - AFE7 FFFF <sub>H</sub>	64 Kbyte	Online Data Acquisition (OLDA)	SRIBE	Access / SRIBE
	AFE8 0000 <sub>H</sub> - AFFF 7FFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AFFF 8000 <sub>H</sub> - AFFF FFFF <sub>H</sub>	32 Kbyte	Boot ROM (BROM)	Access	SRIBE
11	B000 0000 <sub>H</sub> - B000 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU0 DLMU)	Access	Access
	B001 0000 <sub>H</sub> - B001 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU1 DLMU)	Access	Access
	B002 0000 <sub>H</sub> - B002 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU2 DLMU)	Access	Access
	B003 0000 <sub>H</sub> - B003 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU3 DLMU)	Access	Access
	B004 0000 <sub>H</sub> - B007 FFFF <sub>H</sub>	256 Kbyte	LMU (LMU0 LMURAM)	Access	Access
	B008 0000 <sub>H</sub> - B00B FFFF <sub>H</sub>	256 Kbyte	LMU (LMU1 LMURAM)	Access	Access
	B00C 0000 <sub>H</sub> - B00F FFFF <sub>H</sub>	256 Kbyte	LMU (LMU2 LMURAM)	Access	Access
	B010 0000 <sub>H</sub> - B013 FFFF <sub>H</sub>	256 Kbyte	LMU (LMU3 LMURAM)	Access	Access
	B014 0000 <sub>H</sub> - B014 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU4 DLMU)	Access	Access
	B015 0000 <sub>H</sub> - B015 FFFF <sub>H</sub>	64 Kbyte	LMU (CPU5 DLMU)	Access	Access
	B016 0000 <sub>H</sub> - B03F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	B040 0000 <sub>H</sub> - B040 7FFF <sub>H</sub>	32 Kbyte	DAM (DAM0 RAM0)	Access	Access
	B040 8000 <sub>H</sub> - B040 FFFF <sub>H</sub>	32 Kbyte	DAM (DAM0 RAM1)	Access	Access
	B041 0000 <sub>H</sub> - B041 7FFF <sub>H</sub>	32 Kbyte	DAM (DAM1 RAM0)	Access	Access
	B041 8000 <sub>H</sub> - B041 FFFF <sub>H</sub>	32 Kbyte	DAM (DAM1 RAM1)	Access	Access
	B042 0000 <sub>H</sub> - B7FF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE



Table 2-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
	B800 0000 <sub>H</sub> - B800 1FFF <sub>H</sub>	8 Kbyte	MINIMCDS Trace SRAM (TRAM)	Access	Access
	B800 2000 <sub>H</sub> - B8FF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	B900 0000 <sub>H</sub> - B90F FFFF <sub>H</sub>	1 Mbyte	Extension Memory 0 (EMEM0)	Access <sup>3)</sup>	Access <sup>3)</sup>
	B910 0000 <sub>H</sub> - B91F FFFF <sub>H</sub>	1 Mbyte	Extension Memory 1 (EMEM1)	Access <sup>3)</sup>	Access <sup>3)</sup>
	B920 0000 <sub>H</sub> - B92F FFFF <sub>H</sub>	1 Mbyte	Extension Memory 2 (EMEM2)	Access <sup>3)</sup>	Access <sup>3)</sup>
	B930 0000 <sub>H</sub> - B93F FFFF <sub>H</sub>	1 Mbyte	Extension Memory 3 (EMEM3)	Access <sup>3)</sup>	Access <sup>3)</sup>
	B940 0000 <sub>H</sub> - B947 FFFF <sub>H</sub>	512 Kbyte	Extra Trace Memory (XTM) (only 16 Kbyte physical SRAM)	Access	Access
	B948 0000 <sub>H</sub> - BFFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
12	C000 0000 <sub>H</sub> - CFFF FFFF <sub>H</sub>	-	Reserved <sup>6)</sup>	SRIBE	SRIBE
13	D000 0000 <sub>H</sub> - DFFF FFFF <sub>H</sub>	-	Reserved <sup>6)</sup>	SRIBE	SRIBE
14	E000 0000 <sub>H</sub> - EFFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
15	F000 0000 <sub>H</sub> - FFFF FFFF <sub>H</sub>	256 Mbyte	See <a href="#">Table 1-5</a>		

- 1) PCACHE/DCACHE SRAMs (and the corresponding TAG SRAMs) can be only accessed when mapped into the address space (PCACHE / DCACHE disabled. See CPU chapter, register SMACON for details).
- 2) TAG SRAMs are not meant to be used as general SRAMs and can be accessed only with single data access and only with 64 bit aligned address. Mapping of TAG SRAMs in the address map can be used as additional option for memory testing
- 3) The IOC32 and CIF bus masters must be able to access the EMEM via the EMEM BBB interface using the same address as when the EMEM is accessed via the SRI.
- 4) Host Command Sequence Interpreter
- 5) HSM Command Sequence Interpreter
- 6) See also chapter 'CPU, 'Local and Global Addressing' for CPU local views to segment 'C' and segment 'D'.

## 2.5.2 Segment 15

**Table 1-5** shows the address map of segment 'F' as seen from the SRI and SPB bus masters (bus master agents are described in the chapter On Chip Bus System). It describes the mapping of modules to Segment F. The details of the of the module address ranges can be found in the module chapters register overview.

**Figure 1-1** gives an overview about the address mapping of the module address ranges:

Which modules are mapped into the first 16 KB of segment 'F' and can be accessed by the TC1.6E/P with absolute addressing modes (left side)

Examples of covering modules with relative addressing mode (base address +- 32 KB, in the middle)

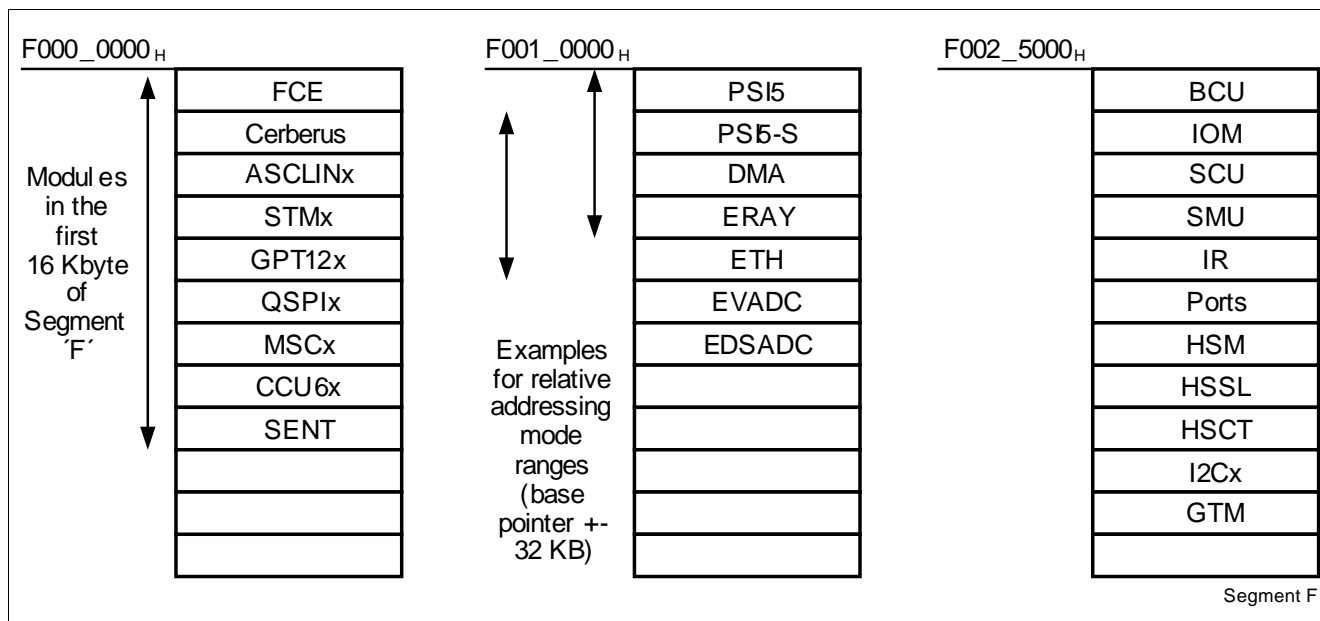


Figure 2-1 Segment F Structure

Table 2-3 On Chip Bus Address Map of Segment 15

Address Range	Size	Unit	Access Type	
			Read	Write
F000_0000 <sub>H</sub> - F000_00FF <sub>H</sub>	256 Byte	Flexible CRC Engine (FCE0) A-Step Silicon only	Access	Access
F000_0100 <sub>H</sub> - F000_03FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000_0000 <sub>H</sub> - F000_01FF <sub>H</sub>	512 Byte	Flexible CRC Engine (FCE0) Productive Silicon Only	Access	Access
F000_0200 <sub>H</sub> - F000_03FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000_0400 <sub>H</sub> - F000_05FF <sub>H</sub>	2 x 256 Byte	On-Chip Debug Support (Cerberus)	Access	Access
F000_0600 <sub>H</sub> - F000_06FF <sub>H</sub>	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 0 (ASCLIN0)	Access	Access
F000_0700 <sub>H</sub> - F000_07FF <sub>H</sub>	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 1 (ASCLIN1)	Access	Access
F000_0800 <sub>H</sub> - F000_08FF <sub>H</sub>	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 2 (ASCLIN2)	Access	Access
F000_0900 <sub>H</sub> - F000_09FF <sub>H</sub>	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 3 (ASCLIN3)	Access	Access
F000_0A00 <sub>H</sub> - F000_0AFF <sub>H</sub>	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 4 (ASCLIN4)	Access	Access
F000_0B00 <sub>H</sub> - F000_0BFF <sub>H</sub>	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 5 (ASCLIN5)	Access	Access
F000_0C00 <sub>H</sub> - F000_0CFF <sub>H</sub>	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 6 (ASCLIN6)	Access	Access
F000_0D00 <sub>H</sub> - F000_0DFF <sub>H</sub>	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 7 (ASCLIN7)	Access	Access



Table 2-3 On Chip Bus Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F000 0E00 <sub>H</sub> - F000 0FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000 1000 <sub>H</sub> - F000 10FF <sub>H</sub>	256 Byte	System Timer 0 (STM0)	Access	Access
F000 1100 <sub>H</sub> - F000 11FF <sub>H</sub>	256 Byte	System Timer 1 (STM1)	Access	Access
F000 1200 <sub>H</sub> - F000 12FF <sub>H</sub>	256 Byte	System Timer 2 (STM2)	Access	Access
F000 1300 <sub>H</sub> - F000 13FF <sub>H</sub>	256 Byte	System Timer 3 (STM3)	Access	Access
F000 1400 <sub>H</sub> - F000 14FF <sub>H</sub>	256 Byte	System Timer 4 (STM4)	Access	Access
F000 1500 <sub>H</sub> - F000 15FF <sub>H</sub>	256 Byte	System Timer 5 (STM5)	Access	Access
F000 1600 <sub>H</sub> - F000 17FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000 1800 <sub>H</sub> - F000 18FF <sub>H</sub>	256 Byte	General Purpose Timer Unit (GPT120)	Access	Access
F000 1900 <sub>H</sub> - F000 1BFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000 1C00 <sub>H</sub> - F000 1CFF <sub>H</sub>	256 Byte	Queued SPI Controller 0 (QSPI0)	Access	Access
F000 1D00 <sub>H</sub> - F000 1DFF <sub>H</sub>	256 Byte	Queued SPI Controller 1 (QSPI1)	Access	Access
F000 1E00 <sub>H</sub> - F000 1EFF <sub>H</sub>	256 Byte	Queued SPI Controller 2 (QSPI2)	Access	Access
F000 1F00 <sub>H</sub> - F000 1FFF <sub>H</sub>	256 Byte	Queued SPI Controller 3 (QSPI3)	Access	Access
F000 2000 <sub>H</sub> - F000 20FF <sub>H</sub>	256 Byte	Queued SPI Controller 4 (QSPI4)	Access	Access
F000 2100 <sub>H</sub> - F000 21FF <sub>H</sub>	256 Byte	Queued SPI Controller 5 (QSPI5)	Access	Access
F000 2200 <sub>H</sub> - F000 25FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000 2600 <sub>H</sub> - F000 26FF <sub>H</sub>	256 Byte	MicroSecond Bus Controller 0 (MSC0)	Access	Access
F000 2700 <sub>H</sub> - F000 27FF <sub>H</sub>	256 Byte	MicroSecond Bus Controller 1 (MSC1)	Access	Access
F000 2800 <sub>H</sub> - F000 28FF <sub>H</sub>	256 Byte	MicroSecond Bus Controller 2 (MSC2)	Access	Access
F000 2900 <sub>H</sub> - F000 29FF <sub>H</sub>	256 Byte	MicroSecond Bus Controller 3 (MSC3)	Access	Access
F000 2A00 <sub>H</sub> - F000 2AFF <sub>H</sub>	256 Byte	Capture/Compare Unit 6 0 (CCU60)	Access	Access
F000 2B00 <sub>H</sub> - F000 2BFF <sub>H</sub>	256 Byte	Capture/Compare Unit 6 1 (CCU61)	Access	Access
F000 2C00 <sub>H</sub> - F000 2FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000 3000 <sub>H</sub> - F000 3AFF <sub>H</sub>	2816 Byte	Single Edge Nibble Transmission (SENT)	Access	Access
F000 3B00 <sub>H</sub> - F000 4FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000 5000 <sub>H</sub> - F000 5AFF <sub>H</sub>	2816 Byte	Peripheral Sensor Interface (PSI5)	Access	Access
F000 5B00 <sub>H</sub> - F000 6FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F000 7000 <sub>H</sub> - F000 7FFF <sub>H</sub>	4 Kbyte	Peripheral Sensor Interface-S (PSI5S)	Access	Access
F000 8000 <sub>H</sub> - F000 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F001 0000 <sub>H</sub> - F001 3FFF <sub>H</sub>	16 Kbyte	Direct Memory Access Controller (DMA)	Access	Access
F001 4000 <sub>H</sub> - F001 6FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F001 7000 <sub>H</sub> - F001 7FFF <sub>H</sub>	4 Kbyte	FlexRay™ Protocol Controller 1 (ERAY1)	Access	Access
F001 8000 <sub>H</sub> - F001 BFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F001 C000 <sub>H</sub> - F001 CFFF <sub>H</sub>	4 Kbyte	FlexRay™ Protocol Controller 0 (ERAY0)	Access	Access

Table 2-3 On Chip Bus Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F001 D000 <sub>H</sub> - F001 D0FF <sub>H</sub>	256 Byte	Ethernet Controller System Control Register (ETH)	Access	Access
F001 D100 <sub>H</sub> - F001 DFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F001 E000 <sub>H</sub> - F001 FFFF <sub>H</sub>	8 Kbyte	Ethernet Controller (ETH)	Access	Access
F002 0000 <sub>H</sub> - F002 3FFF <sub>H</sub>	16 Kbyte	Analog-to-Digital Converter (EVADC)	Access	Access
F002 4000 <sub>H</sub> - F002 4FFF <sub>H</sub>	4 Kbyte	Delta Sigma Analog-to-Digital Converter (EDSADC)	Access	Access
F002 5000 <sub>H</sub> - F002 50FF <sub>H</sub>	256 Byte	Converter Control (CONVCTRL)	Access	Access
F002 5100 <sub>H</sub> - F002 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 0000 <sub>H</sub> - F003 00FF <sub>H</sub>	256 Byte	SPB Bus Control Unit (SBCU)	Access	Access
F003 0100 <sub>H</sub> - F003 4FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 5000 <sub>H</sub> - F003 51FF <sub>H</sub>	2 x 256 Byte	I/O Monitor (IOM0)	Access	Access
F003 5200 <sub>H</sub> - F003 5FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 6000 <sub>H</sub> - F003 63FF <sub>H</sub>	1 Kbyte	System Control Unit (SCU)	Access	Access
F003 6400 <sub>H</sub> - F003 67FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 6800 <sub>H</sub> - F003 6FFF <sub>H</sub>	2 Kbyte	Safety Management Unit (SMU)	Access	Access
F003 7000 <sub>H</sub> - F003 7FFF <sub>H</sub>	4 Kbyte	Interrupt Router (INT)	Access	Access
F003 8000 <sub>H</sub> - F003 9FFF <sub>H</sub>	8 Kbyte	Interrupt Router SRC Registers (INT)	Access	Access
F003 A000 <sub>H</sub> - F003 A0FF <sub>H</sub>	256 Byte	Port 00 (P00)	Access	Access
F003 A100 <sub>H</sub> - F003 A1FF <sub>H</sub>	256 Byte	Port 01 (P01)	Access	Access
F003 A200 <sub>H</sub> - F003 A2FF <sub>H</sub>	256 Byte	Port 02 (P02)	Access	Access
F003 A300 <sub>H</sub> - F003 A9FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 AA00 <sub>H</sub> - F003 AAFF <sub>H</sub>	256 Byte	Port 10 (P10)	Access	Access
F003 AB00 <sub>H</sub> - F003 ABFF <sub>H</sub>	256 Byte	Port 11 (P11)	Access	Access
F003 AC00 <sub>H</sub> - F003 ACFF <sub>H</sub>	256 Byte	Port 12 (P12)	Access	Access
F003 AD00 <sub>H</sub> - F003 ADFF <sub>H</sub>	256 Byte	Port 13 (P13)	Access	Access
F003 AE00 <sub>H</sub> - F003 AEFF <sub>H</sub>	256 Byte	Port 14 (P14)	Access	Access
F003 AF00 <sub>H</sub> - F003 AFFF <sub>H</sub>	256 Byte	Port 15 (P15)	Access	Access
F003 B000 <sub>H</sub> - F003 B3FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 B400 <sub>H</sub> - F003 B4FF <sub>H</sub>	256 Byte	Port 20 (P20)	Access	Access
F003 B500 <sub>H</sub> - F003 B5FF <sub>H</sub>	256 Byte	Port 21 (P21)	Access	Access
F003 B600 <sub>H</sub> - F003 B6FF <sub>H</sub>	256 Byte	Port 22 (P22)	Access	Access
F003 B700 <sub>H</sub> - F003 B7FF <sub>H</sub>	256 Byte	Port 23 (P23)	Access	Access
F003 B800 <sub>H</sub> - F003 B8FF <sub>H</sub>	256 Byte	Port 24 (P24)	Access	Access
F003 B900 <sub>H</sub> - F003 B9FF <sub>H</sub>	256 Byte	Port 25 (P25)	Access	Access
F003 BA00 <sub>H</sub> - F003 BAFF <sub>H</sub>	256 Byte	Port 26 (P26)	Access	Access
F003 BB00 <sub>H</sub> - F003 BDFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 BE00 <sub>H</sub> - F003 BEFF <sub>H</sub>	256 Byte	Port 30 (P30)	Access	Access

Table 2-3 On Chip Bus Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F003 BF00 <sub>H</sub> - F003 BFFF <sub>H</sub>	256 Byte	Port 31 (P31)	Access	Access
F003 C000 <sub>H</sub> - F003 C0FF <sub>H</sub>	256 Byte	Port 32 (P32)	Access	Access
F003 C100 <sub>H</sub> - F003 C1FF <sub>H</sub>	256 Byte	Port 33 (P33)	Access	Access
F003 C200 <sub>H</sub> - F003 C2FF <sub>H</sub>	256 Byte	Port 34 (P34)	Access	Access
F003 C300 <sub>H</sub> - F003 C7FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 C800 <sub>H</sub> - F003 C8FF <sub>H</sub>	256 Byte	Port 40 (P40)	Access	Access
F003 C900 <sub>H</sub> - F003 C9FF <sub>H</sub>	256 Byte	Port 41 (P41)	Access	Access
F003 CA00 <sub>H</sub> - F003 D1FF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F003 D200 <sub>H</sub> - F003 D2FF <sub>H</sub>	256 Byte	Port 50 (P50)	Access	Access
F003 D300 <sub>H</sub> - F003 D3FF <sub>H</sub>	256 Byte	Port 51 (P51)	Access	Access
F003 D400 <sub>H</sub> - F003 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F004 0000 <sub>H</sub> - F005 FFFF <sub>H</sub>	128 Kbyte	Hardware Security Module (HSM)	Access	Access
F006 0000 <sub>H</sub> - F006 FFFF <sub>H</sub>	64 Kbyte	Memory Test Unit (MTU)	Access	Access
F007 0000 <sub>H</sub> - F007 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F008 0000 <sub>H</sub> - F008 03FF <sub>H</sub>	4 x 256 Byte	High Speed Serial Link (HSSL0)	Access	Access
F008 0400 <sub>H</sub> - F008 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F009 0000 <sub>H</sub> - F009 FFFF <sub>H</sub>	64 Kbyte	High Speed Communication Tunnel (HSCT0)	Access	Access
F00A 0000 <sub>H</sub> - F00B FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F00A 0000 <sub>H</sub> - F00A 03FF <sub>H</sub>	4 x 256 Byte	High Speed Serial Link (HSSL1) Productive Silicon Only	SPBBE	SPBBE
F00A 0400 <sub>H</sub> - F00A FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F00B 0000 <sub>H</sub> - F00B FFFF <sub>H</sub>	64 Kbyte	High Speed Communication Tunnel (HSCT1) Productive Silicon Only	SPBBE	SPBBE
F00C 0000 <sub>H</sub> - F00C FFFF <sub>H</sub>	64 Kbyte	I2C0 (I2C0)	Access	Access
F00D 0000 <sub>H</sub> - F00D 00FF <sub>H</sub>	256 Byte	I2C0 System Control Register (I2C0)	Access	Access
F00D 0100 <sub>H</sub> - F00D FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F00E 0000 <sub>H</sub> - F00E FFFF <sub>H</sub>	64 Kbyte	I2C1 (I2C1)	Access	Access
F00F 0000 <sub>H</sub> - F00F 00FF <sub>H</sub>	256 Byte	I2C1 System Control Register (I2C1)	Access	Access
F00F 0100 <sub>H</sub> - F00F FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F010 0000 <sub>H</sub> - F01F FFFF <sub>H</sub>	1 Mbyte	Global Timer Module (GTM)	Access	Access
F020 0000 <sub>H</sub> - F01F FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F020 0000 <sub>H</sub> - F020 7FFF <sub>H</sub>	32 Kbyte	MCMCAN0 SRAM (CAN0)	Access	Access
F020 8000 <sub>H</sub> - F020 8FFF <sub>H</sub>	4 Kbyte	MCMCAN0 SFR (CAN0)	Access	Access
F020 9000 <sub>H</sub> - F020 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F021 0000 <sub>H</sub> - F021 7FFF <sub>H</sub>	32 Kbyte	MCMCAN1 SRAM (CAN1)	Access	Access
F021 8000 <sub>H</sub> - F021 8FFF <sub>H</sub>	4 Kbyte	MCMCAN1 SFR (CAN1)	Access	Access

Table 2-3 On Chip Bus Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F021 9000 <sub>H</sub> - F021 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F022 0000 <sub>H</sub> - F022 7FFF <sub>H</sub>	32 Kbyte	MCMCAN2 SRAM (CAN2)	Access	Access
F022 8000 <sub>H</sub> - F022 8FFF <sub>H</sub>	4 Kbyte	MCMCAN2 SFR (CAN2)	Access	Access
F022 9000 <sub>H</sub> - F023 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F024 0000 <sub>H</sub> - F024 7FFF <sub>H</sub>	32 Kbyte	Standby Controller XRAM (SCR XRAM)	Access	Access
F024 8000 <sub>H</sub> - F024 81FF <sub>H</sub>	512 Byte	Power Management Controller (PMC)	Access	Access
F024 8200 <sub>H</sub> - F7FF 7FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F024 8200 <sub>H</sub> - F027 FFFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F028 0000 <sub>H</sub> - F028 1FFF <sub>H</sub>	8 Kbyte	High Speed Pulse Density Modulation SRAM (HSPDM) Productive Silicon Only	SPBBE	SPBBE
F028 2000 <sub>H</sub> - F028 20FF <sub>H</sub>	256 Byte	High Speed Pulse Density Modulation SFR (HSPDM) Productive Silicon Only	SPBBE	SPBBE
F028 2100 <sub>H</sub> - F7FF 7FFF <sub>H</sub>	—	Reserved	SPBBE	SPBBE
F800 0000 <sub>H</sub> - F801 FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F802 0000 <sub>H</sub> - F802 FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F803 0000 <sub>H</sub> - F803 00FF <sub>H</sub>	256 Byte	FSI SFR (PMU)	Access	Access
F803 0100 <sub>H</sub> - F803 7FFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F803 8000 <sub>H</sub> - F803 FFFF <sub>H</sub>	32 Kbyte	Boot ROM Control (PMU)	Access	Access
F804 0000 <sub>H</sub> - F804 FFFF <sub>H</sub>	64 Kbyte	Host Command Interface (DMU)	Access	Access
F805 0000 <sub>H</sub> - F805 FFFF <sub>H</sub>	64 Kbyte	Host Protection Configuration (DMU)	Access	Access
F806 0000 <sub>H</sub> - F806 FFFF <sub>H</sub>	64 Kbyte	HSM Command Interface (DMU)	Access	Access
F807 0000 <sub>H</sub> - F807 FFFF <sub>H</sub>	64 Kbyte	HSM Protection Configuration (DMU)	Access	Access
F808 0000 <sub>H</sub> - F80F FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F810 0000 <sub>H</sub> - F810 FFFF <sub>H</sub>	64 Kbyte	Local Memory Unit (LMU0)	Access	Access
F811 0000 <sub>H</sub> - F811 FFFF <sub>H</sub>	64 Kbyte	Local Memory Unit (LMU1)	Access	Access
F812 0000 <sub>H</sub> - F812 FFFF <sub>H</sub>	64 Kbyte	Local Memory Unit (LMU2)	Access	Access
F813 0000 <sub>H</sub> - F813 FFFF <sub>H</sub>	64 Kbyte	Local Memory Unit (LMU3)	Access	Access
F814 0000 <sub>H</sub> - F83F FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F840 0000 <sub>H</sub> - F840 FFFF <sub>H</sub>	64 Kbyte	External Bus Unit (EBU0)	Access	Access
F841 0000 <sub>H</sub> - F84F FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F850 0000 <sub>H</sub> - F850 FFFF <sub>H</sub>	64 Kbyte	DAM (DAM0)	Access	Access
F851 0000 <sub>H</sub> - F851 FFFF <sub>H</sub>	64 Kbyte	DAM (DAM1)	Access	Access
F852 0000 <sub>H</sub> - F86F FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F870 0000 <sub>H</sub> - F870 FFFF <sub>H</sub>	64 Kbyte	SRI Domain 0 & 1 SFR (XBAR)	Access	Access
F871 0000 <sub>H</sub> - F87F FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F880 0000 <sub>H</sub> - F880 FFFF <sub>H</sub>	64 Kbyte	CPU0 SFR (CPU0)	Access	Access

Table 2-3 On Chip Bus Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F881 0000 <sub>H</sub> - F881 FFFF <sub>H</sub>	64 Kbyte	CPU0 CSFR (CPU0)	Access	Access
F882 0000 <sub>H</sub> - F882 FFFF <sub>H</sub>	64 Kbyte	CPU1 SFR (CPU1)	Access	Access
F883 0000 <sub>H</sub> - F883 FFFF <sub>H</sub>	64 Kbyte	CPU1 CSFR (CPU1)	Access	Access
F884 0000 <sub>H</sub> - F884 FFFF <sub>H</sub>	64 Kbyte	CPU2 SFR (CPU2)	Access	Access
F885 0000 <sub>H</sub> - F885 FFFF <sub>H</sub>	64 Kbyte	CPU2 CSFR (CPU2)	Access	Access
F886 0000 <sub>H</sub> - F886 FFFF <sub>H</sub>	64 Kbyte	CPU3 SFR (CPU3)	Access	Access
F887 0000 <sub>H</sub> - F887 FFFF <sub>H</sub>	64 Kbyte	CPU3 CSFR (CPU3)	Access	Access
F888 0000 <sub>H</sub> - F888 FFFF <sub>H</sub>	64 Kbyte	CPU4 SFR (CPU4)	Access	Access
F889 0000 <sub>H</sub> - F889 FFFF <sub>H</sub>	64 Kbyte	CPU4 CSFR (CPU4)	Access	Access
F88A 0000 <sub>H</sub> - F88B FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
F88C 0000 <sub>H</sub> - F88C FFFF <sub>H</sub>	64 Kbyte	CPU5 SFR (CPU5)	Access	Access
F88D 0000 <sub>H</sub> - F88D FFFF <sub>H</sub>	64 Kbyte	CPU5 CSFR (CPU5)	Access	Access
F88E 0000 <sub>H</sub> - F9FF FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
FA00 0000 <sub>H</sub> - FA00 00FF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FA00 0100 <sub>H</sub> - FA00 01FF <sub>H</sub>	256 Byte	BBB Bus Control Unit (EBCU)	Access	Access
FA00 0200 <sub>H</sub> - FA00 0FFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FA00 1000 <sub>H</sub> - FA00 10FF <sub>H</sub>	256 Byte	AGBT	Access	Access
FA00 1100 <sub>H</sub> - FA00 1EFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FA00 1F00 <sub>H</sub> - FA00 1FFF <sub>H</sub>	256 Byte	Camera Interface SFR (CIF) A-Step Silicon Only	Access	Access
FA00 2000 <sub>H</sub> - FA00 5FFF <sub>H</sub>	16 Kbyte	Camera Interface RAM (CIF) A-Step Silicon Only	Access	Access
FA00 1100 <sub>H</sub> - FA00 5EFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FA00 6000 <sub>H</sub> - FA00 60FF <sub>H</sub>	256 Byte	EMEM Control Registers	Access	Access
FA00 6100 <sub>H</sub> - FA00 FFFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FA01 0000 <sub>H</sub> - FA01 FFFF <sub>H</sub>	64 Kbyte	MCDS	Access	Access
FA02 0000 <sub>H</sub> - FA03 FFFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FA04 0000 <sub>H</sub> - FA04 01FF <sub>H</sub>	512 Byte	Radar Interface 0 SFR (RIF0)	Access	Access
FA04 0200 <sub>H</sub> - FA04 03FF <sub>H</sub>	512 Byte	Radar Interface 1 SFR (RIF1)	Access	Access
FA04 0400 <sub>H</sub> - FA06 FFFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FA70 0000 <sub>H</sub> - FA70 00FF <sub>H</sub>	256 Byte	SPU Lockstep SFR	Access	Access
FA70 0100 <sub>H</sub> - FA7F FFFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FA80 0000 <sub>H</sub> - FA80 03FF <sub>H</sub>	1 Kbyte	Signal Processing Unit 0 SFR (SPU0)	Access	Access
FA80 0400 <sub>H</sub> - FA9F FFFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FAA0 0000 <sub>H</sub> - FAA0 FFFF <sub>H</sub>	64 Kbyte	SPU0 Configuration RAM (SPUCFG0)	Access	Access
FAA1 0000 <sub>H</sub> - FABF FFFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FAC0 0000 <sub>H</sub> - FAC0 03FF <sub>H</sub>	1 Kbyte	Signal Processing Unit 1 SFR (SPU1)	Access	Access
FAC0 0400 <sub>H</sub> - FADF FFFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE

**Table 2-3 On Chip Bus Address Map of Segment 15 (cont'd)**

Address Range	Size	Unit	Access Type	
			Read	Write
FAE0 0000 <sub>H</sub> - FAE0 FFFF <sub>H</sub>	64 Kbyte	SPU1 Configuration RAM (SPUCFG1)	Access	Access
FAE1 0000 <sub>H</sub> - FAFF FFFF <sub>H</sub>	—	Reserved	BBBBE	BBBBE
FB00 0000 <sub>H</sub> - FB00 FFFF <sub>H</sub>	64 Kbyte	Extension Memory 0 SRI Interface Control SFR (EMEM0)	Access	Access
FB01 0000 <sub>H</sub> - FB01 FFFF <sub>H</sub>	64 Kbyte	Extension Memory 1 SRI Interface Control SFR (EMEM1)	Access	Access
FB02 0000 <sub>H</sub> - FB02 FFFF <sub>H</sub>	64 Kbyte	Extension Memory 2 SRI Interface Control SFR (EMEM2)	Access	Access
FB03 0000 <sub>H</sub> - FB03 FFFF <sub>H</sub>	64 Kbyte	Extension Memory 3 SRI Interface Control SFR (EMEM3)	Access	Access
FB04 0000 <sub>H</sub> - FB6F FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
FB70 0000 <sub>H</sub> - FB70 FFFF <sub>H</sub>	64 Kbyte	SRI ED Domain SFR	Access	Access
FB71 0000 <sub>H</sub> - FB71 7FFF <sub>H</sub>	32 Kbyte	TRAM SFR (TRAM)	Access	Access
FB71 8000 <sub>H</sub> - FB71 FFFF <sub>H</sub>	32 Kbyte	MINIMCDS SFR (MINIMCDS)	Access	Access
FB72 0000 <sub>H</sub> - FBFF FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
FC00 0000 <sub>H</sub> - FFBF FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE
FFC0 0000 <sub>H</sub> - FFC1 FFFF <sub>H</sub>	128 Kbyte	Data Flash 1 EEPROM (DF1) HSM Command Sequence Interpreter	Access	Access <sup>1)</sup>
FFC2 0000 <sub>H</sub> - FFC3 FFFF <sub>H</sub>	128 Kbyte	Reserved	SRIBE	SRIBE
FFC4 0000 <sub>H</sub> - FFFF FFFF <sub>H</sub>	—	Reserved	SRIBE	SRIBE

1) HSM Command Sequence Interpreter

### 2.5.3 Memory Module Access Restrictions

**Table 1-6** describes which type of accesses are possible to the different memories.

**Table 2-4 Possible Memory Accesses<sup>1)</sup>**

Memory		Bit	Byte		Half-word		Word		Double-word	
		rmw	r	w	r	w	r	w	r	w
PMBI <sup>2)</sup>	PSPR	y	y	y	y	y	y	y	y	y
	PTAG <sup>3)</sup>	-	-	-	-	-	y	y	-	-
	PCACHE	y	y	y	y	y	y	y	y	y
DMBI <sup>2)</sup>	DSPR	y	y	y	y	y	y	y	y	y
	DTAG <sup>3)</sup>	-	-	-	-	-	y	y	-	-
	DCACHE	y	y	y	y	y	y	y	y	y
LMU <sup>2)</sup>	LMURAM	y	y	y	y	y	y	y	y	y
	TRAM	y	y	y	y	y	y	y	y	y
PMU	BROM	-	y	-	y	-	y	-	y	-
	PFLASH	-	y	-	y	-	y	y	y	y
	DFLASH	-	y	-	y	-	y	y	y	y