

### 3.3 Address Map of the On Chip Bus System

This chapter describes the system address map as it is seen from the SRI and SPB bus masters (bus master agents are described in the chapter On Chip Bus System).

All bus master agents can address identical peripherals and memories at identical address. The system address map is visible and valid for all CPUs which means that all peripherals and resources are accessible from all TriCore CPUs and other on chip bus master agents.

Parallel access by more than one bus master agents to one slave agent are executed sequentially. Additionally the SRI and SPB bus do support atomic Read Modify Write sequences from the CPUs. Hardware semaphores for temporary exclusive bus access from one master to a slave are not implemented

#### 3.3.1 Segments 0 to 14

**Table 3-2** shows the address map of segments 0 to 14.

**Table 3-2 On Chip Bus Address Map of Segment 0 to 14**

Segment	Address Range	Size	Description	Access Type	
				Read <sup>1)</sup>	Write <sup>2)</sup>
0-4	0000 0000 <sub>H</sub> - 0000 0007 <sub>H</sub>	8 byte	Reserved (virtual address space)	SRIBE	SRIBE
	0000 0008 <sub>H</sub> - 4FFF FFFF <sub>H</sub>	-		SRIBE	SRIBE
5	5000 0000 <sub>H</sub> - 5001 DFFF <sub>H</sub>	120 Kbyte	CPU2 Data Scratch-Pad SRAM (CPU2.DSPR)	access	access
	5001 E000 <sub>H</sub> - 5001 FFFF <sub>H</sub>	8 Kbyte	CPU2. Data Cache SRAM (CPU2.DCACHE)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
	5002 0000 <sub>H</sub> - 500B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	500C 0000 <sub>H</sub> - 500C 0BFF <sub>H</sub>	-	CPU2 Data Cache TAG SRAM <sup>4)</sup> (CPU2.DTAG)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
	500C 0C00 <sub>H</sub> - 500F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	5010 0000 <sub>H</sub> - 5010 7FFF <sub>H</sub>	32 Kbyte	CPU2 Program Scratch-Pad SRAM (CPU2.PSPR)	access	access
	5010 8000 <sub>H</sub> - 5010 BFFF <sub>H</sub>	16 Kbyte	CPU2.Program Cache SRAM (CPU2.PCache)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE

## Memory Maps

Table 3-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Seg- ment	Address Range	Size	Description	Access Type	
				Read <sup>1)</sup>	Write <sup>2)</sup>
6	5010 C000 <sub>H</sub> - 501B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	501C 0000 <sub>H</sub> - 501C 17FF <sub>H</sub>	-	CPU2 Program Cache TAG SRAM <sup>4)</sup> (CPU2.PTAG)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
	501C 1800 <sub>H</sub> - 5FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	6000 0000 <sub>H</sub> - 6001 DFFF <sub>H</sub>	120 Kbyte	CPU1 Data Scratch-Pad SRAM (CPU1.DSPR)	access	access
	6001 E000 <sub>H</sub> - 6001 FFFF <sub>H</sub>	8 Kbyte	CPU1.Data Cache SRAM (CPU1.DCACHE)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
	6002 0000 <sub>H</sub> - 600B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	600C 0000 <sub>H</sub> - 600C 0BFF <sub>H</sub>	-	CPU1 Data Cache TAG SRAM <sup>4)</sup> (CPU1.DTAG)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
	600C 0C00 <sub>H</sub> - 600F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	6010 0000 <sub>H</sub> - 6010 7FFF <sub>H</sub>	32 Kbyte	CPU1 Program Scratch- Pad SRAM (CPU1.PSPR)	access	access
	6010 8000 <sub>H</sub> - 6010 BFFF <sub>H</sub>	16 Kbyte	CPU1.Program Cache SRAM (CPU1.PCache)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
7	6010 C000 <sub>H</sub> - 601B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	601C 0000 <sub>H</sub> - 601C 17FF <sub>H</sub>	-	CPU1 Program Cache TAG SRAM <sup>4)</sup> (CPU1.PTAG)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
	601C 1800 <sub>H</sub> - 6FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	7000 0000 <sub>H</sub> - 7001 BFFF <sub>H</sub>	112 Kbyte	CPU0 Data Scratch-Pad SRAM (CPU0.DSPR)	access	access
	7001 C000 <sub>H</sub> - 700F FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE

**Memory Maps**
**Table 3-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)**

Seg- ment	Address Range	Size	Description	Access Type	
				Read <sup>1)</sup>	Write <sup>2)</sup>
	7010 0000 <sub>H</sub> - 7010 5FFF <sub>H</sub>	24 Kbyte	CPU0 Program Scratch- Pad SRAM (CPU0.PSPR)	access	access
	7010 6000 <sub>H</sub> - 7010 7FFF <sub>H</sub>	8 Kbyte	CPU0.Program Cache SRAM (CPU0.PCache)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
	7010 8000 <sub>H</sub> - 701B FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	701C 0000 <sub>H</sub> - 701C 0BFF <sub>H</sub>	-	CPU0 Program Cache TAG SRAM <sup>4)</sup> (CPU0.PTAG)	access <sup>3)</sup> / SRIBE	access <sup>3)</sup> / SRIBE
	701C 0C00 <sub>H</sub> - 7FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
8	8000 0000 <sub>H</sub> - 801F FFFF <sub>H</sub>	2 Mbyte	Program Flash 0 (PF0)	access	access <sup>2)</sup>
	8020 0000 <sub>H</sub> - 803F FFFF <sub>H</sub>	2 Mbyte	Program Flash 1 (PF1)	access	access <sup>2)</sup>
	8040 0000 <sub>H</sub> - 8FE6 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	8FE7 0000 <sub>H</sub> - 8FE7 7FFF <sub>H</sub>	32 Kbyte	Online Data Acquisition (OLDA)	SRIBE	access <sup>5)</sup> / SRIBE
	8FE7 8000 <sub>H</sub> - 8FFF 7FFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	8FFF 8000 <sub>H</sub> - 8FFF FFFF <sub>H</sub>	32 Kbyte	Boot ROM (BROM)	access	SRIBE
9	9000 0000 <sub>H</sub> - 9000 7FFF <sub>H</sub>	32 Kbyte	LMU SRAM (LMURAM)	access	access
	9000 8000 <sub>H</sub> - 9EFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	9F00 0000 <sub>H</sub> - 9F0F FFFF <sub>H</sub>	1 Mbyte	Reserved for TC27x Emulation Device Memory (EMEM)	SRIBE	SRIBE <sup>6)</sup>
	9F10 0000 <sub>H</sub> - 9FFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE

**Memory Maps**
**Table 3-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)**

Seg- ment	Address Range	Size	Description	Access Type	
				Read <sup>1)</sup>	Write <sup>2)</sup>
10	A000 0000 <sub>H</sub> - A01F FFFF <sub>H</sub>	2 Mbyte	Program Flash 0 (PF0)	access	access <sup>2)</sup>
	A020 0000 <sub>H</sub> - A03F FFFF <sub>H</sub>	2 Mbyte	Program Flash 1 (PF1)	access	access <sup>2)</sup>
	A040 0000 <sub>H</sub> - AEFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AF00 0000 <sub>H</sub> - AF0F FFFF <sub>H</sub>	1 Mbyte	Data Flash 0 (DF0 Address Range)	access	access <sup>2)7)</sup>
	AF10 0000 <sub>H</sub> - AF10 3FFF <sub>H</sub>	16 Kbyte	Data Flash 0 (DF0 Address Range)	access	access <sup>2)7)</sup>
	AF10 4000 <sub>H</sub> - AF10 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AF11 0000 <sub>H</sub> - AF11 FFFF <sub>H</sub>	64 Kbyte	Data Flash 1 (DF1)	access	access <sup>2)</sup>
	AF12 0000 <sub>H</sub> - AFE6 FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AFE7 0000 <sub>H</sub> - AFE7 7FFF <sub>H</sub>	32 Kbyte	Online Data Acquisition (OLDA)	SRIBE	access <sup>5)</sup> / SRIBE
	AFE7 8000 <sub>H</sub> - AFF7 7FFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	AFFF 8000 <sub>H</sub> - AFFF FFFF <sub>H</sub>	32 Kbyte	Boot ROM (BROM)	access	SRIBE
11	B000 0000 <sub>H</sub> - B000 7FFF <sub>H</sub>	32 Kbyte	LMU SRAM (LMURAM)	access	access
	B000 8000 <sub>H</sub> - BEFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
	BF00 0000 <sub>H</sub> - BF0F FFFF <sub>H</sub>	1 MB	Reserved for TC27x Emulation Device Memory (EMEM)	SRIBE	SRIBE <sup>6)</sup>
	BF10 0000 <sub>H</sub> - BFFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
12	C000 0000 <sub>H</sub> - CFFF FFFF <sub>H</sub>	-	Reserved <sup>8)</sup>	SRIBE	SRIBE

**Memory Maps**
**Table 3-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)**

Segment	Address Range	Size	Description	Access Type	
				Read <sup>1)</sup>	Write <sup>2)</sup>
13	D000 0000 <sub>H</sub> - DFFF FFFF <sub>H</sub>	-	Reserved <sup>8)</sup>	SRIBE	SRIBE
14	E000 0000 <sub>H</sub> - EFFF FFFF <sub>H</sub>	-	Reserved	SRIBE	SRIBE
15	F000 0000 <sub>H</sub> - FFFF FFFF <sub>H</sub>	256 Mbyte	see <a href="#">Table 3-3</a>		

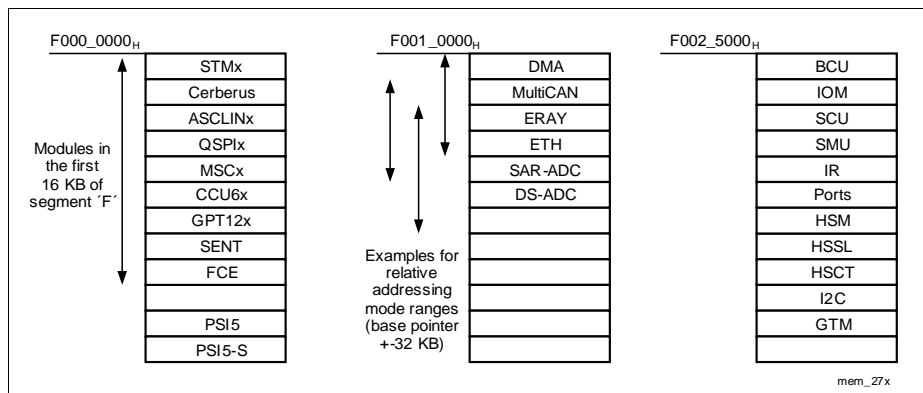
- 1) A read transaction through the SRI to FPI bridge that is terminated with Bus Error will result in Bus Errors on SRI and FPI (valid for transactions from FPI to SRI and SRI to FPI).
- 2) Write access to Flash resources are handled by the PMU module (Flash command sequence, see PMU chapter for details).
- 3) PCache/DCache SRAMs (and the corresponding TAG SRAMs) can be only accessed when mapped into the address space (PCache / DCache disabled. See MTU chapter, register MTU\_MEMMAP for details).
- 4) TAG SRAMs are not meant to be used as general SRAMs and can be accessed only with single data access and only with 64 bit aligned address. Mapping of TAG SRAMs in the address map can be used as additional option for memory testing.
- 5) Online Data Acquisition address space can be disabled/enabled via LMU control register bit LMU\_MEMCON.OLDAEN. TC1.6P access to OLDA address space via segment 8 (cached) results in SRIBE independent of the LMU\_MEMCON.OLDAEN bit setting.
- 6) This address range is mapped to the LMU module. A read/write from/to this address range will result in an SRI Bus Error initiated by the LMU module.
- 7) DF0 is the address where all Data Flash blocks are mapped to. The details about the Data Flash block sizes, segmentation and exact mapping are described in the chapter PMU.
- 8) See also chapter 'CPU, 'Local and Global Addressing' for CPU local views to segment 'C' and segment 'D'.

### 3.3.2 Segment 15

**Table 3-3** shows the address map of segment 'F' as seen from the SRI and SPB bus masters (bus master agents are described in the chapter On Chip Bus System).

**Table 3-1** gives an overview about the address mapping of the module address ranges:

- which modules are mapped into the first 16 KB of segment 'F' and can be accessed by the TC1.6E/P with absolute addressing modes (left side)
- examples of covering modules with relative addressing mode (base address +- 32 KB, in the middle)



**Figure 3-1 Segment F Structure**

Please note that **Table 3-3** describes the mapping of modules to segment F. The details of the module address ranges can be found in the module chapters register overview.

**Table 3-3 On Chip Bus Address Map of Segment 15**

Unit	Address Range	Size	Access Type	
			Read	Write
System Timer 0 (STM0)	F000 0000 <sub>H</sub> - F000 00FF <sub>H</sub>	256 byte	access	access
System Timer 1 (STM1)	F000 0100 <sub>H</sub> - F000 01FF <sub>H</sub>	256 byte	access	access
System Timer 2 (STM2)	F000 0200 <sub>H</sub> - F000 02FF <sub>H</sub>	256 byte	access	access
Reserved	F000 0300 <sub>H</sub> - F000 03FF <sub>H</sub>	–	SPBBE	SPBBE

**Memory Maps**
**Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)**

Unit	Address Range	Size	Access Type	
			Read	Write
On-Chip Debug Support (Cerberus)	F000 0400 <sub>H</sub> - F000 05FF <sub>H</sub>	2x256 byte	access	access
ASCLIN0 (ASCLIN0)	F000 0600 <sub>H</sub> - F000 06FF <sub>H</sub>	256 byte	access	access
ASCLIN1 (ASCLIN1)	F000 0700 <sub>H</sub> - F000 07FF <sub>H</sub>	256 byte	access	access
ASCLIN2 (ASCLIN2)	F000 0800 <sub>H</sub> - F000 08FF <sub>H</sub>	256 byte	access	access
ASCLIN3 (ASCLIN3)	F000 0900 <sub>H</sub> - F000 09FF <sub>H</sub>	256 byte	access	access
Reserved	F000 0A00 <sub>H</sub> - F000 1BFF <sub>H</sub>	–	SPBBE	SPBBE
QUEUED SPI 0 (QSPI0)	F000 1C00 <sub>H</sub> - F000 1CFF <sub>H</sub>	256 byte	access	access
QUEUED SPI 1 (QSPI1)	F000 1D00 <sub>H</sub> - F000 1DFF <sub>H</sub>	256 byte	access	access
QUEUED SPI 2 (QSPI2)	F000 1E00 <sub>H</sub> - F000 1EFF <sub>H</sub>	256 byte	access	access
QUEUED SPI 3 (QSPI3)	F000 1F00 <sub>H</sub> - F000 1FFF <sub>H</sub>	256 byte	access	access
Reserved	F000 2000 <sub>H</sub> - F000 25FF <sub>H</sub>	–	SPBBE	SPBBE
MicroSecond Bus Controller 0 (MSC0)	F000 2600 <sub>H</sub> - F000 26FF <sub>H</sub>	256 byte	access	access
MicroSecond Bus Controller 1 (MSC1)	F000 2700 <sub>H</sub> - F000 27FF <sub>H</sub>	256 byte	access	access
Reserved	F000 2800 <sub>H</sub> - F000 29FF <sub>H</sub>	–	SPBBE	SPBBE
Capture/Compare Unit 6 0 (CCU60)	F000 2A00 <sub>H</sub> - F000 2AFF <sub>H</sub>	256 byte	access	access
Capture/Compare Unit 6 1 (CCU61)	F000 2B00 <sub>H</sub> - F000 2BFF <sub>H</sub>	256 byte	access	access

## Memory Maps

**Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)**

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	F000 2C00 <sub>H</sub> - F000 2DFF <sub>H</sub>	–	SPBBE	SPBBE
General Purpose Timer 12 0 (GPT120)	F000 2E00 <sub>H</sub> - F000 2EFF <sub>H</sub>	256 byte	access	access
Reserved	F000 2F00 <sub>H</sub> - F000 2FFF <sub>H</sub>	–	SPBBE	SPBBE
SENT Module (SENT)	F000 3000 <sub>H</sub> - F000 3AFF <sub>H</sub>	11x256 byte	access	access
Reserved	F000 3B00 <sub>H</sub> - F000 3EFF <sub>H</sub>	–	SPBBE	SPBBE
Flexible CRC Engine (FCE)	F000 3F00 <sub>H</sub> - F000 3FFF <sub>H</sub>	256 byte	access	access
Reserved	F000 4000 <sub>H</sub> - F000 4FFF <sub>H</sub>	–	SPBBE	SPBBE
PSI5 (PSI5)	F000 5000 <sub>H</sub> - F000 6FFF <sub>H</sub>	8 KByte	access	access
PSI5-S (PSI5-S)	F000 7000 <sub>H</sub> - F000 7FFF <sub>H</sub>	4 KByte	access	access
Reserved	F000 8000 <sub>H</sub> - F000 FFFF <sub>H</sub>	–	SPBBE	SPBBE
Direct Memory Access Controller (DMA)	F001 0000 <sub>H</sub> - F001 3FFF <sub>H</sub>	16 KByte	access	access
Reserved	F001 4000 <sub>H</sub> - F001 7FFF <sub>H</sub>	–	SPBBE	SPBBE
MultiCAN Controller (CAN)	F001 8000 <sub>H</sub> - F001 BFFF <sub>H</sub>	16 Kbyte	access	access
FlexRay™ Protocol Controller (E-Ray)	F001 C000 <sub>H</sub> - F001 CFFF <sub>H</sub>	4 Kbyte	access	access
Ethernet Controller System Control Register (ETH)	F001 D000 <sub>H</sub> - F001 D0FF <sub>H</sub>	256 byte	access	access
Reserved	F001 D100 <sub>H</sub> - F001 DFFF <sub>H</sub>	–	SPBBE	SPBBE



## Memory Maps

**Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)**

Unit	Address Range	Size	Access Type	
			Read	Write
Ethernet Controller (ETH)	F001 E000 <sub>H</sub> - F001 FFFF <sub>H</sub>	8 KByte	access	access
Analog-to-Digital Converter (VADC)	F002 0000 <sub>H</sub> - F002 3FFF <sub>H</sub>	16 KByte	access	access
Delta Sigma Ditigal Analog-to-Digital Converter (DSADC)	F002 4000 <sub>H</sub> - F002 4FFF <sub>H</sub>	4 Kbyte	access	access
Reserved	F002 5000 <sub>H</sub> - F002 FFFF <sub>H</sub>	–	SPBBE	SPBBE
System Peripheral Bus Control Unit (BCU)	F003 0000 <sub>H</sub> - F003 00FF <sub>H</sub>	256 byte	access	access
Reserved	F003 0100 <sub>H</sub> - F003 4FFF <sub>H</sub>	–	SPBBE	SPBBE
I/O Monitor (IOM)	F003 5000 <sub>H</sub> - F003 51FF <sub>H</sub>	2x256 byte	access	access
Reserved	F003 5200 <sub>H</sub> - F003 5FFF <sub>H</sub>	–	SPBBE	SPBBE
System Control Unit (SCU)	F003 6000 <sub>H</sub> - F003 63FF <sub>H</sub>	1 Kbyte	access	access
Reserved	F003 6400 <sub>H</sub> - F003 67FF <sub>H</sub>	–	SPBBE	SPBBE
Safety Management Unit (SMU)	F003 6800 <sub>H</sub> - F003 6FFF <sub>H</sub>	2 Kbyte	access	access
Interrupt Router (IR)	F003 7000 <sub>H</sub> - F003 7FFF <sub>H</sub>	4 Kbyte	access	access
Interrupt Router (IR) SRC Registers	F003 8000 <sub>H</sub> - F003 9FFF <sub>H</sub>	8 Kbyte	access	access
Port 00	F003 A000 <sub>H</sub> - F003 A0FF <sub>H</sub>	256 byte	access	access
Port 01	F003 A100 <sub>H</sub> - F003 A1FF <sub>H</sub>	256 byte	access	access
Port 02	F003 A200 <sub>H</sub> - F003 A2FF <sub>H</sub>	256 byte	access	access

## Memory Maps

**Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)**

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	F003 A300 <sub>H</sub> - F003 AFFF <sub>H</sub>	–	SPBBE	SPBBE
Port 10	F003 B000 <sub>H</sub> - F003 B0FF <sub>H</sub>	256 byte	access	access
Port 11	F003 B100 <sub>H</sub> - F003 B1FF <sub>H</sub>	256 byte	access	access
Port 12	F003 B200 <sub>H</sub> - F003 B2FF <sub>H</sub>	256 byte	access	access
Port 13	F003 B300 <sub>H</sub> - F003 B3FF <sub>H</sub>	256 byte	access	access
Port 14	F003 B400 <sub>H</sub> - F003 B4FF <sub>H</sub>	256 byte	access	access
Port 15	F003 B500 <sub>H</sub> - F003 B5FF <sub>H</sub>	256 byte	access	access
Reserved	F003 B600 <sub>H</sub> - F003 BFFF <sub>H</sub>	–	SPBBE	SPBBE
Port 20	F003 C000 <sub>H</sub> - F003 C0FF <sub>H</sub>	256 byte	access	access
Port 21	F003 C100 <sub>H</sub> - F003 C1FF <sub>H</sub>	256 byte	access	access
Port 22	F003 C200 <sub>H</sub> - F003 C2FF <sub>H</sub>	256 byte	access	access
Port 23	F003 C300 <sub>H</sub> - F003 C3FF <sub>H</sub>	256 byte	access	access
Reserved	F003 C400 <sub>H</sub> - F003 D1FF <sub>H</sub>	–	SPBBE	SPBBE
Port 32	F003 D200 <sub>H</sub> - F003 D2FF <sub>H</sub>	256 byte	access	access
Port 33	F003 D300 <sub>H</sub> - F003 D3FF <sub>H</sub>	256 byte	access	access
Port 34	F003 D400 <sub>H</sub> - F003 D4FF <sub>H</sub>	256 byte	access	access

**Memory Maps**
**Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)**

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	F003 D500 <sub>H</sub> - F003 DFFF <sub>H</sub>	–	SPBBE	SPBBE
Port 40	F003 E000 <sub>H</sub> - F003 E0FF <sub>H</sub>	256 byte	access	access
Reserved	F003 E100 <sub>H</sub> - F003 FFFF <sub>H</sub>	–	SPBBE	SPBBE
High Security Module (HSM)	F004 0000 <sub>H</sub> - F005 FFFF <sub>H</sub>	128 Kbyte	access	access
Memory Test Unit (MTU)	F006 0000 <sub>H</sub> - F006 FFFF <sub>H</sub>	64 Kbyte	access	access
Reserved	F007 0000 <sub>H</sub> - F007 FFFF <sub>H</sub>	–	SPBBE	SPBBE
High Speed Serial Link (HSSL)	F008 0000 <sub>H</sub> - F008 03FF <sub>H</sub>	4x256 byte	access	access
Reserved	F008 0400 <sub>H</sub> - F008 FFFF <sub>H</sub>	–	SPBBE	SPBBE
High Speed Communication Tunnel (HSCT)	F009 0000 <sub>H</sub> - F009 FFFF <sub>H</sub>	64 Kbyte	access	access
Reserved	F00A 0000 <sub>H</sub> - F00B FFFF <sub>H</sub>	–	SPBBE	SPBBE
I2C 0 (I2C0)	F00C 0000 <sub>H</sub> - F00C FFFF <sub>H</sub>	64 Kbyte	access	access
I2C 0 System Control Register (I2C0)	F00D 0000 <sub>H</sub> - F00D 00FF <sub>H</sub>	256 byte	access	access
Reserved	F00D 0100 <sub>H</sub> - F00F FFFF <sub>H</sub>	–	SPBBE	SPBBE
Global Timer Module (GTM)	F010 0000 <sub>H</sub> - F019 FFFF <sub>H</sub>	640 Kbyte	access	access
Reserved	F01A 0000 <sub>H</sub> - F7FF FFFF <sub>H</sub>	–	SPBBE	SPBBE
Reserved	F800 0000 <sub>H</sub> - F800 04FF <sub>H</sub>	–	SRIBE	SRIBE

## Memory Maps

**Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)**

Unit	Address Range	Size	Access Type	
			Read	Write
Program Memory Unit 0 (PMU0)	F800 0500 <sub>H</sub> - F800 05FF <sub>H</sub>	256 byte	access	access
Reserved	F800 0600 <sub>H</sub> - F800 0FFF <sub>H</sub>	–	SRIBE	SRIBE
Flash Register (PMU0)	F800 1000 <sub>H</sub> - F800 23FF <sub>H</sub>	5 Kbyte	access	access
Reserved	F800 2400 <sub>H</sub> - F86F FFFF <sub>H</sub>	–	SRIBE	SRIBE
SRI Crossbar (XBar_SRI)	F870 0000 <sub>H</sub> - F870 04FF <sub>H</sub>	5x256 byte	access	access
Reserved	F870 0500 <sub>H</sub> - F870 07FF <sub>H</sub>	–	SRIBE	SRIBE
Local Memory Unit (LMU)	F870 0800 <sub>H</sub> - F870 08FF <sub>H</sub>	256 byte	access	access
DAM Unit (DAM)	F870 0900 <sub>H</sub> - F870 0BFF <sub>H</sub>	3x256 byte	access	access
Reserved	F870 0C00 <sub>H</sub> - F87F FFFF <sub>H</sub>	–	SRIBE	SRIBE
CPU0 SFR	F880 0000 <sub>H</sub> - F880 FFFF <sub>H</sub>	64 KByte	access	access
CPU0 CSFR	F881 0000 <sub>H</sub> - F881 FFFF <sub>H</sub>	64 KByte	access	access
CPU1 SFR	F882 0000 <sub>H</sub> - F882 FFFF <sub>H</sub>	64 KByte	access	access
CPU1 CSFR	F883 0000 <sub>H</sub> - F883 FFFF <sub>H</sub>	64 KByte	access	access
CPU2 SFR	F884 0000 <sub>H</sub> - F884 FFFF <sub>H</sub>	64 KByte	access	access
CPU2 CSFR	F885 0000 <sub>H</sub> - F885 FFFF <sub>H</sub>	64 KByte	access	access
Reserved	F886 0000 <sub>H</sub> - F8FF FFFF <sub>H</sub>	–	SRIBE	SRIBE

## Memory Maps

**Table 3-3 On Chip Bus Address Map of Segment 15 (cont'd)**

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved for TC27x Emulation Device Registers (ED Reg)	F900 0000 <sub>H</sub> - F90F FFFF <sub>H</sub>	1 MB	access	access
Reserved	F910 0000 <sub>H</sub> - FF10 FFFF <sub>H</sub>	–	SRIBE	SRIBE
HSM	FF11 0000 <sub>H</sub> - FF11 FFFF <sub>H</sub>	64 KByte	access	access
Reserved	FF12 0000 <sub>H</sub> - FFFF FFFF <sub>H</sub>	–	SRIBE	SRIBE