

Memory Maps (MEMMAP)

Segment 11

This memory segment allows non-cached access to LMU and to EMEM.

Segment 12

This memory segment is reserved.

Segment 13

This memory segment is reserved.

Segment 14

This memory segment is reserved.

Segment 15

The lower 128 Mbyte is SPB address space and the upper 128 Mbyte is SRI address space.

2.3.2 Address Map of the On Chip Bus System

All bus master agents can address identical peripherals and memories at identical addresses. The system address map is visible and valid for all CPUs which means that all peripherals and resources are accessible from all TriCore CPUs and other on chip bus master agents.

Parallel access by more than one bus master agent to one slave agent are executed sequentially. Additionally the SRI, SPB and BBB support atomic Read Modify Write sequences from the CPUs.

2.3.2.1 Segments 0 to 14

Table 17 shows the address map of segments 0 to 14.

Notes

1. *Write Access Type: Write access to Flash resources are handled by the DMU module (Flash command sequence, see DMU chapter for details).*

Table 17 Address Map of Segment 0 to 14

Segment	Address Range	Size	Description	Access Type	
				Read	Write
0	0000 0000 _H - 0000 0007 _H	8 Byte	Reserved (virtual address space)	SRIBE / SPBBE ¹⁾	SRIBE / SPBBE ¹⁾
	0000 0008 _H - 0FFF FFFF _H	-	Reserved	SRIBE	SRIBE
1	1000 0000 _H - 1001 7FFF _H	96 Kbyte	CPU5 Data Scratch-Pad SRAM (CPU5 DSPR)	Access	Access
	1001 8000 _H - 1001 BFFF _H	16 Kbyte	CPU5. Data Cache SRAM (CPU5 DCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	1001 C000 _H - 100B FFFF _H	-	Reserved	SRIBE	SRIBE
	100C 0000 _H - 100C 17FF _H	-	CPU5 Data Cache TAG SRAM ³⁾ (CPU5 DTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	100C 1800 _H - 100F FFFF _H	-	Reserved	SRIBE	SRIBE

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Table 17 Address Map of Segment 0 to 14 (cont'd)

Segm ent	Address Range	Size	Description	Access Type	
				Read	Write
	1010 0000 _H - 1010 FFFF _H	64 Kbyte	CPU5 Program Scratch-Pad SRAM (CPU5 PSPR)	Access	Access
	1011 0000 _H - 1011 7FFF _H	32 Kbyte	CPU5.Program Cache SRAM (CPU5 PCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	1011 8000 _H - 101B FFFF _H	-	Reserved	SRIBE	SRIBE
	101C 0000 _H - 101C 2FFF _H	-	CPU5 Program Cache TAG SRAM ³⁾ (CPU5 PTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	101C 3000 _H - 1FFF FFFF _H	-	Reserved	SRIBE	SRIBE
2	2000 0000 _H - 2FFF FFFF _H	-	Reserved	SRIBE	SRIBE
3	3000 0000 _H - 3001 7FFF _H	96 Kbyte	CPU4 Data Scratch-Pad SRAM (CPU4 DSPR)	Access	Access
	3001 8000 _H - 3001 BFFF _H	16 Kbyte	CPU4. Data Cache SRAM (CPU4 DCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	3001 C000 _H - 300B FFFF _H	-	Reserved	SRIBE	SRIBE
	300C 0000 _H - 300C 17FF _H	-	CPU4 Data Cache TAG SRAM ¹⁾ (CPU4 DTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	300C 1800 _H - 300F FFFF _H	-	Reserved	SRIBE	SRIBE
	3010 0000 _H - 3010 FFFF _H	64 Kbyte	CPU4 Program Scratch-Pad SRAM (CPU4 PSPR)	Access	Access
	3011 0000 _H - 3011 7FFF _H	32 Kbyte	CPU4.Program Cache SRAM (CPU4 PCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	3011 8000 _H - 301B FFFF _H	-	Reserved	SRIBE	SRIBE
	301C 0000 _H - 301C 2FFF _H	-	CPU4 Program Cache TAG SRAM ¹⁾ (CPU4 PTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	301C 3000 _H - 3FFF FFFF _H	-	Reserved	SRIBE	SRIBE
4	4000 0000 _H - 4001 7FFF _H	96 Kbyte	CPU3 Data Scratch-Pad SRAM (CPU3 DSPR)	Access	Access
	4001 8000 _H - 4001 BFFF _H	16 Kbyte	CPU3. Data Cache SRAM (CPU3 DCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	4001 C000 _H - 400B FFFF _H	-	Reserved	SRIBE	SRIBE
	400C 0000 _H - 400C 17FF _H	-	CPU3 Data Cache TAG SRAM ¹⁾ (CPU3 DTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	400C 1800 _H - 400F FFFF _H	-	Reserved	SRIBE	SRIBE
	4010 0000 _H - 4010 FFFF _H	64 Kbyte	CPU3 Program Scratch-Pad SRAM (CPU3 PSPR)	Access	Access
	4011 0000 _H - 4011 7FFF _H	32 Kbyte	CPU3.Program Cache SRAM (CPU3 PCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	4011 8000 _H - 401B FFFF _H	-	Reserved	SRIBE	SRIBE
	401C 0000 _H - 401C 2FFF _H	-	CPU3 Program Cache TAG SRAM ¹⁾ (CPU3 PTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE

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Table 17 Address Map of Segment 0 to 14 (cont'd)

Segm ent	Address Range	Size	Description	Access Type	
				Read	Write
5	401C 3000 _H - 4FFF FFFF _H	-	Reserved	SRIBE	SRIBE
	5000 0000 _H - 5001 7FFF _H	96 Kbyte	CPU2 Data Scratch-Pad SRAM (CPU2 DSPR)	Access	Access
	5001 8000 _H - 5001 BFFF _H	16 Kbyte	CPU2. Data Cache SRAM (CPU2 DCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	5001 C000 _H - 500B FFFF _H	-	Reserved	SRIBE	SRIBE
	500C 0000 _H - 500C 17FF _H	-	CPU2 Data Cache TAG SRAM ¹⁾ (CPU2 DTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	500C 1800 _H - 500F FFFF _H	-	Reserved	SRIBE	SRIBE
	5010 0000 _H - 5010 FFFF _H	64 Kbyte	CPU2 Program Scratch-Pad SRAM (CPU2 PSPR)	Access	Access
	5011 0000 _H - 5011 7FFF _H	32 Kbyte	CPU2.Program Cache SRAM (CPU2 PCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	5011 8000 _H - 501B FFFF _H	-	Reserved	SRIBE	SRIBE
	501C 0000 _H - 501C 2FFF _H	-	CPU2 Program Cache TAG SRAM ¹⁾ (CPU2 PTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
6	501C 3000 _H - 5FFF FFFF _H	-	Reserved	SRIBE	SRIBE
	6000 0000 _H - 6003 BFFF _H	240 Kbyte	CPU1 Data Scratch-Pad SRAM (CPU1 DSPR)	Access	Access
	6003 C000 _H - 6003 FFFF _H	16 Kbyte	CPU1. Data Cache SRAM (CPU1 DCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	6004 0000 _H - 600B FFFF _H	-	Reserved	SRIBE	SRIBE
	600C 0000 _H - 600C 17FF _H	-	CPU1 Data Cache TAG SRAM ¹⁾ (CPU1 DTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	600C 1800 _H - 600F FFFF _H	-	Reserved	SRIBE	SRIBE
	6010 0000 _H - 6010 FFFF _H	64 Kbyte	CPU1 Program Scratch-Pad SRAM (CPU1 PSPR)	Access	Access
	6011 0000 _H - 6011 7FFF _H	32 Kbyte	CPU1.Program Cache SRAM (CPU1 PCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	6011 8000 _H - 601B FFFF _H	-	Reserved	SRIBE	SRIBE
	601C 0000 _H - 601C 2FFF _H	-	CPU1 Program Cache TAG SRAM ¹⁾ (CPU1 PTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
7	601C 3000 _H - 6FFF FFFF _H	-	Reserved	SRIBE	SRIBE
	7000 0000 _H - 7003 BFFF _H	240 Kbyte	CPU0 Data Scratch-Pad SRAM (CPU0 DSPR)	Access	Access
	7003 C000 _H - 7003 FFFF _H	16 Kbyte	CPU0. Data Cache SRAM (CPU0 DCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	7004 0000 _H - 700B FFFF _H	-	Reserved	SRIBE	SRIBE
	700C 0000 _H - 700C 17FF _H	-	CPU0 Data Cache TAG SRAM ¹⁾ (CPU0 DTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE

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Table 17 Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
	700C 1800 _H - 700F FFFF _H	-	Reserved	SRIBE	SRIBE
	7010 0000 _H - 7010 FFFF _H	64 Kbyte	CPU0 Program Scratch-Pad SRAM (CPU0 PSPR)	Access	Access
	7011 0000 _H - 7011 7FFF _H	32 Kbyte	CPU0.Program Cache SRAM (CPU0 PCACHE)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	7011 8000 _H - 701B FFFF _H	-	Reserved	SRIBE	SRIBE
	701C 0000 _H - 701C 2FFF _H	-	CPU0 Program Cache TAG SRAM ¹⁾ (CPU0 PTAG)	Access ²⁾ / SRIBE	Access ²⁾ / SRIBE
	701C 3000 _H - 7FFF FFFF _H	-	Reserved	SRIBE	SRIBE
8	8000 0000 _H - 802F FFFF _H	3 Mbyte	Program Flash 0 (PF0)	Access	SRIBE
	8030 0000 _H - 805F FFFF _H	3 Mbyte	Program Flash 1 (PF1)	Access	SRIBE
	8060 0000 _H - 808F FFFF _H	3 Mbyte	Program Flash 2 (PF2)	Access	SRIBE
	8090 0000 _H - 80BF FFFF _H	3 Mbyte	Program Flash 3 (PF3)	Access	SRIBE
	80C0 0000 _H - 80EF FFFF _H	3 Mbyte	Program Flash 4 (PF4)	Access	SRIBE
	80F0 0000 _H - 80FF FFFF _H	1 Mbyte	Program Flash 5 (PF5)	Access	SRIBE
	8100 0000 _H - 811F FFFF _H	2 Mbyte	Reserved (for PFLASH)	SRIBE	SRIBE
	8120 0000 _H - 81FF FFFF _H	-	Reserved	SRIBE	SRIBE
	8200 0000 _H - 87FF FFFF _H	96 Mbyte	External Bus Unit (EBU)	Access	Access
	8800 0000 _H - 8FDF FFFF _H	-	Reserved	SRIBE	SRIBE
	8FE0 0000 _H - 8FE7 FFFF _H	512 Kbyte	Online Data Acquisition (OLDA)	SRIBE	Access / SRIBE
	8FE8 0000 _H - 8FFE FFFF _H	-	Reserved	SRIBE	SRIBE
	8FFF 0000 _H - 8FFF FFFF _H	64 Kbyte	Boot ROM (BROM)	Access	SRIBE
9	9000 0000 _H - 9000 FFFF _H	64 Kbyte	LMU (CPU0 DLMU)	Access	Access
	9001 0000 _H - 9001 FFFF _H	64 Kbyte	LMU (CPU1 DLMU)	Access	Access
	9002 0000 _H - 9002 FFFF _H	64 Kbyte	LMU (CPU2 DLMU)	Access	Access
	9003 0000 _H - 9003 FFFF _H	64 Kbyte	LMU (CPU3 DLMU)	Access	Access
	9004 0000 _H - 9007 FFFF _H	256 Kbyte	LMU (LMU0 LMURAM)	Access	Access
	9008 0000 _H - 900B FFFF _H	256 Kbyte	LMU (LMU1 LMURAM)	Access	Access
	900C 0000 _H - 900F FFFF _H	256 Kbyte	LMU (LMU2 LMURAM)	Access	Access
	9010 0000 _H - 9010 FFFF _H	64 Kbyte	LMU (CPU4 DLMU)	Access	Access
	9011 0000 _H - 9011 FFFF _H	64 Kbyte	LMU (CPU5 DLMU)	Access	Access
	9012 0000 _H - 903F FFFF _H	-	Reserved	SRIBE	SRIBE
	9040 0000 _H - 9040 7FFF _H	32 Kbyte	DAM (DAM0 RAM0)	Access	Access
	9040 8000 _H - 9040 FFFF _H	32 Kbyte	DAM (DAM0 RAM1)	Access	Access
	9041 0000 _H - 9041 7FFF _H	32 Kbyte	DAM (DAM1 RAM0)	Access	Access
	9041 8000 _H - 9041 FFFF _H	32 Kbyte	DAM (DAM1 RAM1)	Access	Access
	9042 0000 _H - 97FF FFFF _H	-	Reserved	SRIBE	SRIBE

Memory Maps (MEMMAP)

Table 17 Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
10	9800 0000 _H - 9800 1FFF _H	8 Kbyte	MINIMCDS Trace SRAM (TRAM)	Access ⁴⁾	Access ⁴⁾
	9800 2000 _H - 98FF FFFF _H	-	Reserved	SRIBE	SRIBE
	9900 0000 _H - 990F FFFF _H	1 Mbyte	EMEM (EMEM Module 0)	Access	Access
	9910 0000 _H - 991F FFFF _H	1 Mbyte	EMEM (EMEM Module 1)	Access	Access
	9920 0000 _H - 992F FFFF _H	1 Mbyte	EMEM (EMEM Module 2)	Access	Access
	9930 0000 _H - 993F FFFF _H	1 Mbyte	EMEM (EMEM Module 3)	Access	Access
	9940 0000 _H - 9FFF FFFF _H	-	Reserved	SRIBE	SRIBE
	A000 0000 _H - A02F FFFF _H	3 Mbyte	Program Flash 0 (PF0)	Access	SRIBE
	A030 0000 _H - A05F FFFF _H	3 Mbyte	Program Flash 1 (PF1)	Access	SRIBE
	A060 0000 _H - A08F FFFF _H	3 Mbyte	Program Flash 2 (PF2)	Access	SRIBE
	A090 0000 _H - A0BF FFFF _H	3 Mbyte	Program Flash 3 (PF3)	Access	SRIBE
	A0C0 0000 _H - A0EF FFFF _H	3 Mbyte	Program Flash 4 (PF4)	Access	SRIBE
	A0F0 0000 _H - A0FF FFFF _H	1 Mbyte	Program Flash 5 (PF5)	Access	SRIBE
	A100 0000 _H - A11F FFFF _H	2 Mbyte	Reserved (for PFLASH)	SRIBE	SRIBE
	A120 0000 _H - A1FF FFFF _H	-	Reserved	SRIBE	SRIBE
	A200 0000 _H - A7FF FFFF _H	96 Mbyte	External Bus Unit (EBU)	Access	Access
	A800 0000 _H - A800 3FFF _H	16 Kbyte	Erase Counter 0 (EC0)	Access	SRIBE
	A800 4000 _H - A807 FFFF _H	-	Reserved	SRIBE	SRIBE
	A808 0000 _H - A80B FFFF _H	256 Kbyte	PFI User Registers 0 (PFI0)	Access	SRIBE
	A80C 0000 _H - A82F FFFF _H	-	Reserved	SRIBE	SRIBE
	A830 0000 _H - A830 3FFF _H	16 Kbyte	Erase Counter 1 (EC1)	Access	SRIBE
	A830 4000 _H - A837 FFFF _H	-	Reserved	SRIBE	SRIBE
	A838 0000 _H - A83B FFFF _H	256 Kbyte	PFI User Registers 1 (PFI1)	Access	SRIBE
	A83C 0000 _H - A85F FFFF _H	-	Reserved	SRIBE	SRIBE
	A860 0000 _H - A860 3FFF _H	16 Kbyte	Erase Counter 2 (EC2)	Access	SRIBE
	A860 4000 _H - A867 FFFF _H	-	Reserved	SRIBE	SRIBE
	A868 0000 _H - A86B FFFF _H	256 Kbyte	PFI User Registers 2 (PFI2)	Access	SRIBE
	A86C 0000 _H - A88F FFFF _H	-	Reserved	SRIBE	SRIBE
	A890 0000 _H - A890 3FFF _H	16 Kbyte	Erase Counter 3 (EC3)	Access	SRIBE
	A890 4000 _H - A897 FFFF _H	-	Reserved	SRIBE	SRIBE
	A898 0000 _H - A89B FFFF _H	256 Kbyte	PFI User Registers 3 (PFI3)	Access	SRIBE
	A89C 0000 _H - A8BF FFFF _H	-	Reserved	SRIBE	SRIBE
	A8C0 0000 _H - A8C0 3FFF _H	16 Kbyte	Erase Counter 4 (EC4)	Access	SRIBE
	A8C0 4000 _H - A8C7 FFFF _H	-	Reserved	SRIBE	SRIBE
	A8C8 0000 _H - A8CB FFFF _H	256 Kbyte	PFI User Registers 4 (PFI4)	Access	SRIBE
	A8CC 0000 _H - A8EF FFFF _H	-	Reserved	SRIBE	SRIBE
	A8F0 0000 _H - A8F0 3FFF _H	16 Kbyte	Erase Counter 5 (EC5)	Access	SRIBE

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Table 17 Address Map of Segment 0 to 14 (cont'd)

Segm ent	Address Range	Size	Description	Access Type	
				Read	Write
	A8F0 4000 _H - A8F7 FFFF _H	-	Reserved	SRIBE	SRIBE
	A8F8 0000 _H - A8FB FFFF _H	256 Kbyte	PFI User Registers 5 (PFI5)	Access	SRIBE
	A8FC 0000 _H - AEFF FFFF _H	-	Reserved	SRIBE	SRIBE
	AF00 0000 _H - AF0F FFFF _H	1 Mbyte	Data Flash 0 EEPROM (DF0) Host Comd. Sequence Interpreter	Access	Access ⁵⁾
	AF10 0000 _H - AF3F FFFF _H	3 Mbyte	Reserved	SRIBE	SRIBE
	AF40 0000 _H - AF40 5FFF _H	24 Kbyte	Data Flash 0 UCB (DF0)	Access	SRIBE
	AF40 6000 _H - AF7F FFFF _H	-	Reserved	SRIBE	SRIBE
	AF80 0000 _H - AF80 FFFF _H	64 Kbyte	Data Flash 0 CFS (DF0)	Access	SRIBE
	AF81 0000 _H - AFBF FFFF _H	-	Reserved	SRIBE	SRIBE
	AFC0 0000 _H - AFC1 FFFF _H	128 Kbyte	Data Flash 1 EEPROM (DF1) HSM Comd. Sequence Interpreter	Access	Access ⁶⁾
	AFC2 0000 _H - AFC3 FFFF _H	128 Kbyte	Reserved	SRIBE	SRIBE
	AFC4 0000 _H - AFDF FFFF _H	-	Reserved	SRIBE	SRIBE
	AFE0 0000 _H - AFE7 FFFF _H	512 Kbyte	Online Data Acquisition (OLDA)	SRIBE	Access / SRIBE
	AFE8 0000 _H - AFFE FFFF _H	-	Reserved	SRIBE	SRIBE
	AFFF 0000 _H - AFFF FFFF _H	64 Kbyte	Boot ROM (BROM)	Access	SRIBE
11	B000 0000 _H - B000 FFFF _H	64 Kbyte	LMU (CPU0 DLMU)	Access	Access
	B001 0000 _H - B001 FFFF _H	64 Kbyte	LMU (CPU1 DLMU)	Access	Access
	B002 0000 _H - B002 FFFF _H	64 Kbyte	LMU (CPU2 DLMU)	Access	Access
	B003 0000 _H - B003 FFFF _H	64 Kbyte	LMU (CPU3 DLMU)	Access	Access
	B004 0000 _H - B007 FFFF _H	256 Kbyte	LMU (LMU0 LMURAM)	Access	Access
	B008 0000 _H - B00B FFFF _H	256 Kbyte	LMU (LMU1 LMURAM)	Access	Access
	B00C 0000 _H - B00F FFFF _H	256 Kbyte	LMU (LMU2 LMURAM)	Access	Access
	B010 0000 _H - B010 FFFF _H	64 Kbyte	LMU (CPU4 DLMU)	Access	Access
	B011 0000 _H - B011 FFFF _H	64 Kbyte	LMU (CPU5 DLMU)	Access	Access
	B012 0000 _H - B03F FFFF _H	-	Reserved	SRIBE	SRIBE
	B040 0000 _H - B040 7FFF _H	32 Kbyte	DAM (DAM0 RAM0)	Access	Access
	B040 8000 _H - B040 FFFF _H	32 Kbyte	DAM (DAM0 RAM1)	Access	Access
	B041 0000 _H - B041 7FFF _H	32 Kbyte	DAM (DAM1 RAM0)	Access	Access
	B041 8000 _H - B041 FFFF _H	32 Kbyte	DAM (DAM1 RAM1)	Access	Access
	B042 0000 _H - B7FF FFFF _H	-	Reserved	SRIBE	SRIBE
	B800 0000 _H - B800 1FFF _H	8 Kbyte	MINIMCDS Trace SRAM (TRAM)	Access ⁴⁾	Access ⁴⁾
	B800 2000 _H - B8FF FFFF _H	-	Reserved	SRIBE	SRIBE
	B900 0000 _H - B90F FFFF _H	1 Mbyte	EMEM (EMEM Module 0)	Access	Access
	B910 0000 _H - B91F FFFF _H	1 Mbyte	EMEM (EMEM Module 1)	Access	Access

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Table 17 Address Map of Segment 0 to 14 (cont'd)

Segm ent	Address Range	Size	Description	Access Type	
				Read	Write
	B920 0000 _H - B92F FFFF _H	1 Mbyte	EMEM (EMEM Module 2)	Access	Access
	B930 0000 _H - B93F FFFF _H	1 Mbyte	EMEM (EMEM Module 3)	Access	Access
	B940 0000 _H - B947 FFFF _H	512 Kbyte	Extra Trace Memory (XTM) (only 16 Kbyte physical SRAM)	Access	Access
	B948 0000 _H - BFFF FFFF _H	-	Reserved	SRIBE	SRIBE
12	C000 0000 _H - CFFF FFFF _H	-	Reserved ⁷⁾	SRIBE	SRIBE
13	D000 0000 _H - DFFF FFFF _H	-	Reserved ⁷⁾	SRIBE	SRIBE
14	E000 0000 _H - EFFF FFFF _H	-	Reserved	SRIBE	SRIBE
15	F000 0000 _H - FFFF FFFF _H	256 Mbyte	See Table 21		

- 1) If an SPB access to 0000 0000_H occurs, the SPB BCU generates a bus error.
- 2) PCACHE/DCACHE SRAMs (and the corresponding TAG SRAMs) can be only accessed when mapped into the address space (PCACHE / DCACHE disabled. See CPU chapter, register SMACON for details).
- 3) TAG SRAMs are not meant to be used as general SRAMs and can be accessed only with single data access and only with 64 bit aligned address. Mapping of TAG SRAMs in the address map can be used as additional option for memory testing
- 4) TRAM shall not be used as a general SRAM and can only be accessed when OCDS is enabled.
- 5) Host Command Sequence Interpreter
- 6) HSM Command Sequence Interpreter
- 7) See also chapter 'CPU, 'Local and Global Addressing' for CPU local views to segment 'C' and segment 'D'.

Table 18 TC39x and TC38x Alternate Address Map for SOTA of Segment 8 PFLASH

Segm ent	Address Range	Size	Description	Access Type	
				Read	Write
8	8000 0000 _H - 802F FFFF _H	3 Mbyte	Program Flash 2 (PF2)	Access	SRIBE
	8030 0000 _H - 805F FFFF _H	3 Mbyte	Program Flash 3 (PF3)	Access	SRIBE
	8060 0000 _H - 808F FFFF _H	3 Mbyte	Program Flash 0 (PF0)	Access	SRIBE
	8090 0000 _H - 80BF FFFF _H	3 Mbyte	Program Flash 1 (PF1)	Access	SRIBE
	80C0 0000 _H - 80CF FFFF _H	1 Mbyte	Program Flash 5 (PF5)	Access	SRIBE
	80D0 0000 _H - 80EF FFFF _H	2 Mbyte	Reserved (for PFLASH)	SRIBE	SRIBE
	80F0 0000 _H - 811F FFFF _H	3 Mbyte	Program Flash 4 (PF4)	Access	SRIBE
	8120 0000 _H - 81FF FFFF _H	-	Reserved	SRIBE	SRIBE

Table 19 TC39x and TC38x Alternate Address Map for SOTA of Segment 10 PFLASH

Segm ent	Address Range	Size	Description	Access Type	
				Read	Write
10	A000 0000 _H - A02F FFFF _H	3 Mbyte	Program Flash 2 (PF2)	Access	SRIBE
	A030 0000 _H - A05F FFFF _H	3 Mbyte	Program Flash 3 (PF3)	Access	SRIBE
	A060 0000 _H - A08F FFFF _H	3 Mbyte	Program Flash 0 (PF0)	Access	SRIBE
	A090 0000 _H - A0BF FFFF _H	3 Mbyte	Program Flash 1 (PF1)	Access	SRIBE
	A0C0 0000 _H - A0CF FFFF _H	1 Mbyte	Program Flash 5 (PF5)	Access	SRIBE

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Table 19 TC39x and TC38x Alternate Address Map for SOTA (cont'd) of Segment 10 PFLASH

Segm ent	Address Range	Size	Description	Access Type	
				Read	Write
	A0D0 0000 _H - A0EF FFFF _H	2 Mbyte	Reserved (for PFLASH)	SRIBE	SRIBE
	A0F0 0000 _H - A11F FFFF _H	3 Mbyte	Program Flash 4 (PF4)	Access	SRIBE
	A120 0000 _H - A1FF FFFF _H	-	Reserved	SRIBE	SRIBE

Table 20 TC39x and TC38x Alternate Address Map for SOTA of Segment 10 Erase Counters and Registers

Segm ent	Address Range	Size	Description	Access Type	
				Read	Write
10	A800 0000 _H - A800 3FFF _H	16 Kbyte	Erase Counter 2 (EC2)	Access	SRIBE
	A800 4000 _H - A807 FFFF _H	-	Reserved	SRIBE	SRIBE
	A808 0000 _H - A80B FFFF _H	256 Kbyte	PFI User Registers 2 (PFI2)	Access	SRIBE
	A80C 0000 _H - A82F FFFF _H	-	Reserved	SRIBE	SRIBE
	A830 0000 _H - A830 3FFF _H	16 Kbyte	Erase Counter 3 (EC3)	Access	SRIBE
	A830 4000 _H - A837 FFFF _H	-	Reserved	SRIBE	SRIBE
	A838 0000 _H - A83B FFFF _H	256 Kbyte	PFI User Registers 3 (PFI3)	Access	SRIBE
	A83C 0000 _H - A85F FFFF _H	-	Reserved	SRIBE	SRIBE
	A860 0000 _H - A860 3FFF _H	16 Kbyte	Erase Counter 0 (EC0)	Access	SRIBE
	A860 4000 _H - A867 FFFF _H	-	Reserved	SRIBE	SRIBE
	A868 0000 _H - A86B FFFF _H	256 Kbyte	PFI User Registers 0 (PFI0)	Access	SRIBE
	A86C 0000 _H - A88F FFFF _H	-	Reserved	SRIBE	SRIBE
	A890 0000 _H - A890 3FFF _H	16 Kbyte	Erase Counter 1 (EC1)	Access	SRIBE
	A890 4000 _H - A897 FFFF _H	-	Reserved	SRIBE	SRIBE
	A898 0000 _H - A89B FFFF _H	256 Kbyte	PFI User Registers 1 (PFI1)	Access	SRIBE
	A89C 0000 _H - A8BF FFFF _H	-	Reserved	SRIBE	SRIBE
	A8C0 0000 _H - A8C0 3FFF _H	16 Kbyte	Erase Counter 5 (EC5)	Access	SRIBE
	A8C0 4000 _H - A8C7 FFFF _H	-	Reserved	SRIBE	SRIBE
	A8C8 0000 _H - A8CB FFFF _H	256 Kbyte	PFI User Registers 5 (PFI5)	Access	SRIBE
	A8CC 0000 _H - A8EF FFFF _H	-	Reserved	SRIBE	SRIBE
	A8F0 0000 _H - A8F0 3FFF _H	16 Kbyte	Erase Counter 4 (EC4)	Access	SRIBE
	A8F0 4000 _H - A8F7 FFFF _H	-	Reserved	SRIBE	SRIBE
	A8F8 0000 _H - A8FB FFFF _H	256 Kbyte	PFI User Registers 4 (PFI4)	Access	SRIBE
	A8FC 0000 _H - AEFF FFFF _H	-	Reserved	SRIBE	SRIBE

2.3.2.2 Segment 15

Table 21 shows the address map of segment 'F' as seen from the SRI and SPB bus masters (bus master agents are described in the chapter On Chip Bus System). It describes the mapping of modules to Segment F. The details of the module address ranges can be found in the module chapters register overview.

Figure 14 gives an overview about the address mapping of the module address ranges:

- Absolute Addressing Range

Memory Maps (MEMMAP)

- If a module is addressed in the first 16 Kbyte of segment 'F', the CPU can access the module with absolute addressing mode.
- Others
 - If a module is addressed above the first 16 Kbyte of segment 'F', the CPU can access the module with base + offset.

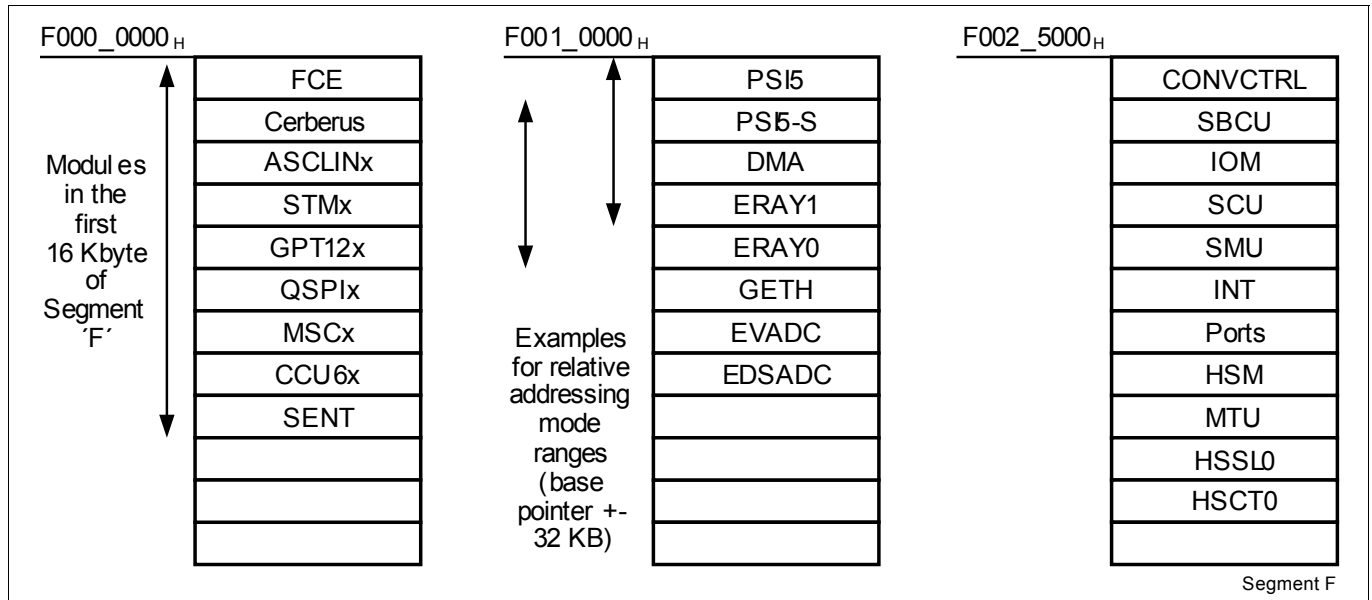


Figure 14 Segment F Structure

Table 21 Address Map of Segment 15

Address Range	Size	Unit	Access Type	
			Read	Write
F000 0000 _H - F000 01FF _H	512 Byte	Flexible CRC Engine (FCE0)	Access	Access
F000 0200 _H - F000 03FF _H	–	Reserved	SPBBE	SPBBE
F000 0400 _H - F000 05FF _H	2 x 256 Byte	On-Chip Debug Support (Cerberus)	Access	Access
F000 0600 _H - F000 06FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 0 (ASCLIN0)	Access	Access
F000 0700 _H - F000 07FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 1 (ASCLIN1)	Access	Access
F000 0800 _H - F000 08FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 2 (ASCLIN2)	Access	Access
F000 0900 _H - F000 09FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 3 (ASCLIN3)	Access	Access
F000 0A00 _H - F000 0AFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 4 (ASCLIN4)	Access	Access
F000 0B00 _H - F000 0BFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 5 (ASCLIN5)	Access	Access
F000 0C00 _H - F000 0CFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 6 (ASCLIN6)	Access	Access

Memory Maps (MEMMAP)

Table 21 Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F000 0D00 _H - F000 0DFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 7 (ASCLIN7)	Access	Access
F000 0E00 _H - F000 0EFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 8 (ASCLIN8)	Access	Access
F000 0F00 _H - F000 0FFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 9 (ASCLIN9)	Access	Access
F000 1000 _H - F000 10FF _H	256 Byte	System Timer 0 (STM0)	Access	Access
F000 1100 _H - F000 11FF _H	256 Byte	System Timer 1 (STM1)	Access	Access
F000 1200 _H - F000 12FF _H	256 Byte	System Timer 2 (STM2)	Access	Access
F000 1300 _H - F000 13FF _H	256 Byte	System Timer 3 (STM3)	Access	Access
F000 1400 _H - F000 14FF _H	256 Byte	System Timer 4 (STM4)	Access	Access
F000 1500 _H - F000 15FF _H	256 Byte	System Timer 5 (STM5)	Access	Access
F000 1600 _H - F000 17FF _H	–	Reserved	SPBBE	SPBBE
F000 1800 _H - F000 18FF _H	256 Byte	General Purpose Timer Unit (GPT120)	Access	Access
F000 1900 _H - F000 1BFF _H	–	Reserved	SPBBE	SPBBE
F000 1C00 _H - F000 1CFF _H	256 Byte	Queued SPI Controller 0 (QSPI0)	Access	Access
F000 1D00 _H - F000 1DFF _H	256 Byte	Queued SPI Controller 1 (QSPI1)	Access	Access
F000 1E00 _H - F000 1EFF _H	256 Byte	Queued SPI Controller 2 (QSPI2)	Access	Access
F000 1F00 _H - F000 1FFF _H	256 Byte	Queued SPI Controller 3 (QSPI3)	Access	Access
F000 2000 _H - F000 20FF _H	256 Byte	Queued SPI Controller 4 (QSPI4)	Access	Access
F000 2100 _H - F000 21FF _H	256 Byte	Queued SPI Controller 5 (QSPI5)	Access	Access
F000 2200 _H - F000 25FF _H	–	Reserved	SPBBE	SPBBE
F000 2600 _H - F000 26FF _H	256 Byte	MicroSecond Bus Controller 0 (MSC0)	Access	Access
F000 2700 _H - F000 27FF _H	256 Byte	MicroSecond Bus Controller 1 (MSC1)	Access	Access
F000 2800 _H - F000 28FF _H	256 Byte	MicroSecond Bus Controller 2 (MSC2)	Access	Access
F000 2900 _H - F000 29FF _H	256 Byte	MicroSecond Bus Controller 3 (MSC3)	Access	Access
F000 2A00 _H - F000 2AFF _H	256 Byte	Capture/Compare Unit 6 0 (CCU60)	Access	Access
F000 2B00 _H - F000 2BFF _H	256 Byte	Capture/Compare Unit 6 1 (CCU61)	Access	Access
F000 2C00 _H - F000 2FFF _H	–	Reserved	SPBBE	SPBBE
F000 3000 _H - F000 3AFF _H	11 x 256 Byte	Single Edge Nibble Transmission (SENT)	Access	Access
F000 3B00 _H - F000 4FFF _H	–	Reserved	SPBBE	SPBBE
F000 5000 _H - F000 5AFF _H	11 x 256 Byte	Peripheral Sensor Interface (PSI5)	Access	Access
F000 5B00 _H - F000 6FFF _H	–	Reserved	SPBBE	SPBBE
F000 7000 _H - F000 7FFF _H	4 Kbyte	Peripheral Sensor Interface-S (PSI5S)	Access	Access
F000 8000 _H - F000 FFFF _H	–	Reserved	SPBBE	SPBBE
F001 0000 _H - F001 3FFF _H	16 Kbyte	Direct Memory Access Controller (DMA)	Access	Access
F001 4000 _H - F001 6FFF _H	–	Reserved	SPBBE	SPBBE

Memory Maps (MEMMAP)

Table 21 Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F001 7000 _H - F001 7FFF _H	4 Kbyte	FlexRay™ Protocol Controller 1 (ERAY1)	Access	Access
F001 8000 _H - F001 BFFF _H	–	Reserved	SPBBE	SPBBE
F001 C000 _H - F001 CFFF _H	4 Kbyte	FlexRay™ Protocol Controller 0 (ERAY0)	Access	Access
F001 D000 _H - F001 DFFF _H	4 Kbyte	Gigabit Ethernet Controller MAC Control (GETH)	Access	Access
F001 E000 _H - F001 EFFF _H	4 Kbyte	Gigabit Ethernet Controller DMA Control (GETH)	Access	Access
F001 F000 _H - F001 F0FF _H	256 Byte	Gigabit Ethernet Controller SFR (GETH)	Access	Access
F001 F100 _H - F001 FFFF _H	–	Reserved	SPBBE	SPBBE
F002 0000 _H - F002 3FFF _H	16 Kbyte	Analog-to-Digital Converter (EVADC)	Access	Access
F002 4000 _H - F002 4FFF _H	4 Kbyte	Delta Sigma Analog-to-Digital Converter (EDSADC)	Access	Access
F002 5000 _H - F002 50FF _H	256 Byte	Converter Control (CONVCTRL)	Access	Access
F002 5100 _H - F002 FFFF _H	–	Reserved	SPBBE	SPBBE
F003 0000 _H - F003 00FF _H	256 Byte	SPB Bus Control Unit (SBCU)	Access	Access
F003 0100 _H - F003 4FFF _H	–	Reserved	SPBBE	SPBBE
F003 5000 _H - F003 51FF _H	2 x 256 Byte	I/O Monitor (IOM)	Access	Access
F003 5200 _H - F003 5FFF _H	–	Reserved	SPBBE	SPBBE
F003 6000 _H - F003 63FF _H	1 Kbyte	System Control Unit (SCU)	Access	Access
F003 6400 _H - F003 67FF _H	–	Reserved	SPBBE	SPBBE
F003 6800 _H - F003 6FFF _H	2 Kbyte	Safety Management Unit (SMU)	Access	Access
F003 7000 _H - F003 7FFF _H	4 Kbyte	Interrupt Router (INT)	Access	Access
F003 8000 _H - F003 9FFF _H	8 Kbyte	Interrupt Router SRC Registers (INT)	Access	Access
F003 A000 _H - F003 A0FF _H	256 Byte	Port 00 (P00)	Access	Access
F003 A100 _H - F003 A1FF _H	256 Byte	Port 01 (P01)	Access	Access
F003 A200 _H - F003 A2FF _H	256 Byte	Port 02 (P02)	Access	Access
F003 A300 _H - F003 A9FF _H	–	Reserved	SPBBE	SPBBE
F003 AA00 _H - F003 AAFF _H	256 Byte	Port 10 (P10)	Access	Access
F003 AB00 _H - F003 ABFF _H	256 Byte	Port 11 (P11)	Access	Access
F003 AC00 _H - F003 ACFF _H	256 Byte	Port 12 (P12)	Access	Access
F003 AD00 _H - F003 ADFF _H	256 Byte	Port 13 (P13)	Access	Access
F003 AE00 _H - F003 AEFF _H	256 Byte	Port 14 (P14)	Access	Access
F003 AF00 _H - F003 AFFF _H	256 Byte	Port 15 (P15)	Access	Access
F003 B000 _H - F003 B3FF _H	–	Reserved	SPBBE	SPBBE
F003 B400 _H - F003 B4FF _H	256 Byte	Port 20 (P20)	Access	Access
F003 B500 _H - F003 B5FF _H	256 Byte	Port 21 (P21)	Access	Access
F003 B600 _H - F003 B6FF _H	256 Byte	Port 22 (P22)	Access	Access

Memory Maps (MEMMAP)

Table 21 Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F003 B700 _H - F003 B7FF _H	256 Byte	Port 23 (P23)	Access	Access
F003 B800 _H - F003 B8FF _H	256 Byte	Port 24 (P24)	Access	Access
F003 B900 _H - F003 B9FF _H	256 Byte	Port 25 (P25)	Access	Access
F003 BA00 _H - F003 BAFF _H	256 Byte	Port 26 (P26)	Access	Access
F003 BB00 _H - F003 BDFF _H	–	Reserved	SPBBE	SPBBE
F003 BE00 _H - F003 BEFF _H	256 Byte	Port 30 (P30)	Access	Access
F003 BF00 _H - F003 BFFF _H	256 Byte	Port 31 (P31)	Access	Access
F003 C000 _H - F003 C0FF _H	256 Byte	Port 32 (P32)	Access	Access
F003 C100 _H - F003 C1FF _H	256 Byte	Port 33 (P33)	Access	Access
F003 C200 _H - F003 C2FF _H	256 Byte	Port 34 (P34)	Access	Access
F003 C300 _H - F003 C7FF _H	–	Reserved	SPBBE	SPBBE
F003 C800 _H - F003 C8FF _H	256 Byte	Port 40 (P40)	Access	Access
F003 C900 _H - F003 C9FF _H	256 Byte	Port 41 (P41)	Access	Access
F003 CA00 _H - F003 FFFF _H	–	Reserved	SPBBE	SPBBE
F004 0000 _H - F005 FFFF _H	128 Kbyte	Hardware Security Module (HSM)	Access	Access
F006 0000 _H - F006 FFFF _H	64 Kbyte	Memory Test Unit (MTU)	Access	Access
F007 0000 _H - F007 FFFF _H	–	Reserved	SPBBE	SPBBE
F008 0000 _H - F008 03FF _H	4 x 256 Byte	High Speed Serial Link (HSSL0)	Access	Access
F008 0400 _H - F008 FFFF _H	–	Reserved	SPBBE	SPBBE
F009 0000 _H - F009 FFFF _H	64 Kbyte	High Speed Communication Tunnel (HSCT0)	Access	Access
F00A 0000 _H - F00A 03FF _H	4 x 256 Byte	High Speed Serial Link (HSSL1)	Access	Access
F00A 0400 _H - F00A FFFF _H	–	Reserved	SPBBE	SPBBE
F00B 0000 _H - F00B FFFF _H	64 Kbyte	High Speed Communication Tunnel (HSCT1)	Access	Access
F00C 0000 _H - F00C FFFF _H	64 Kbyte	I2C0 (I2C0)	Access	Access
F00D 0000 _H - F00D 00FF _H	256 Byte	I2C0 System Control Register (I2C0)	Access	Access
F00D 0100 _H - F00D FFFF _H	–	Reserved	SPBBE	SPBBE
F00E 0000 _H - F00E FFFF _H	64 Kbyte	I2C1 (I2C1)	Access	Access
F00F 0000 _H - F00F 00FF _H	256 Byte	I2C1 System Control Register (I2C1)	Access	Access
F00F 0100 _H - F00F FFFF _H	–	Reserved	SPBBE	SPBBE
F010 0000 _H - F01F FFFF _H	1 Mbyte	Generic Timer Module (GTM)	Access	Access
F020 0000 _H - F020 7FFF _H	32 Kbyte	MCMCAN0 SRAM (CAN0)	Access	Access
F020 8000 _H - F020 8FFF _H	4 Kbyte	MCMCAN0 SFR (CAN0)	Access	Access
F020 9000 _H - F020 FFFF _H	–	Reserved	SPBBE	SPBBE
F021 0000 _H - F021 3FFF _H	16 Kbyte	MCMCAN1 SRAM (CAN1)	Access	Access
F021 4000 _H - F021 7FFF _H	–	Reserved	SPBBE	SPBBE

Memory Maps (MEMMAP)

Table 21 Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F021 8000 _H - F021 8FFF _H	4 Kbyte	MCMCAN1 SFR (CAN1)	Access	Access
F021 9000 _H - F021 FFFF _H	–	Reserved	SPBBE	SPBBE
F022 0000 _H - F022 3FFF _H	16 Kbyte	MCMCAN2 SRAM (CAN2)	Access	Access
F022 4000 _H - F022 7FFF _H	–	Reserved	SPBBE	SPBBE
F022 8000 _H - F022 8FFF _H	4 Kbyte	MCMCAN2 SFR (CAN2)	Access	Access
F022 9000 _H - F023 FFFF _H	–	Reserved	SPBBE	SPBBE
F024 0000 _H - F024 1FFF _H	8 Kbyte	Standby Controller XRAM (SCR XRAM)	Access	Access
F024 2000 _H - F024 7FFF _H	–	Reserved	SPBBE	SPBBE
F024 8000 _H - F024 81FF _H	512 Byte	Power Management System (PMS)	Access	Access
F024 8200 _H - F027 FFFF _H	–	Reserved	SPBBE	SPBBE
F028 0000 _H - F028 1FFF _H	8 Kbyte	High Speed Pulse Density Modulation SRAM (HSPDM)	SPBBE	SPBBE
F028 2000 _H - F028 20FF _H	256 Byte	High Speed Pulse Density Modulation SFR (HSPDM)	SPBBE	SPBBE
F028 2100 _H - F02A FFFF _H	–	Reserved	SPBBE	SPBBE
F02B 0000 _H - F02B 0FFF _H	4 Kbyte	Secure Digital Multi Media Card (SDMMC0)	Access	Access
F02B 0200 _H - F02C 09FF _H	–	Reserved	SPBBE	SPBBE
F02C 0A00 _H - F02C 0AFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 10 (ASCLIN10)	Access	Access
F02C 0B00 _H - F02C 0BFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 11 (ASCLIN11)	Access	Access
F02C 0C00 _H - F02C 0CFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 12 (ASCLIN12) ¹⁾	Access	Access
F02C 0D00 _H - F02C 0DFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 13 (ASCLIN13) ¹⁾	Access	Access
F02C 0E00 _H - F02C 0EFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 14 (ASCLIN14) ¹⁾	Access	Access
F02C 0F00 _H - F02C 0FFF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 15 (ASCLIN15) ¹⁾	Access	Access
F02C 1000 _H - F02C 10FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 16 (ASCLIN16) ¹⁾	Access	Access
F02C 1100 _H - F02C 11FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 17 (ASCLIN17) ¹⁾	Access	Access
F02C 1200 _H - F02C 12FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 18 (ASCLIN18) ¹⁾	Access	Access
F02C 1300 _H - F02C 13FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 19 (ASCLIN19) ¹⁾	Access	Access
F02C 1400 _H - F02C 14FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 20 (ASCLIN20) ¹⁾	Access	Access

Memory Maps (MEMMAP)

Table 21 Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F02C 1500 _H - F02C 15FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 21 (ASCLIN21) ¹⁾	Access	Access
F02C 1600 _H - F02C 16FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 22 (ASCLIN22) ¹⁾	Access	Access
F02C 1700 _H - F02C 17FF _H	256 Byte	Asynchronous/Synchronous Serial Controller with LIN 23 (ASCLIN23) ¹⁾	Access	Access
F02C 1800 _H - F7FF FFFF _H	–	Reserved	SPBBE	SPBBE
F800 0000 _H - F801 FFFF _H	–	Reserved	SRIBE	SRIBE
F802 0000 _H - F802 FFFF _H	–	Reserved	SRIBE	SRIBE
F803 0000 _H - F803 00FF _H	256 Byte	FSI SFR (DMU)	Access	Access
F803 0100 _H - F803 7FFF _H	–	Reserved	SRIBE	SRIBE
F803 8000 _H - F803 FFFF _H	32 Kbyte	Boot ROM Control (DMU)	Access	Access
F804 0000 _H - F804 FFFF _H	64 Kbyte	Host Command Interface (DMU)	Access	Access
F805 0000 _H - F805 FFFF _H	64 Kbyte	Host Protection Configuration (DMU)	Access	Access
F806 0000 _H - F806 FFFF _H	64 Kbyte	HSM Command Interface (DMU)	Access	Access
F807 0000 _H - F807 FFFF _H	64 Kbyte	HSM Protection Configuration (DMU)	Access	Access
F808 0000 _H - F80F FFFF _H	–	Reserved	SRIBE	SRIBE
F810 0000 _H - F810 FFFF _H	64 Kbyte	Local Memory Unit (LMU0)	Access	Access
F811 0000 _H - F811 FFFF _H	64 Kbyte	Local Memory Unit (LMU1)	Access	Access
F812 0000 _H - F812 FFFF _H	64 Kbyte	Local Memory Unit (LMU2)	Access	Access
F813 0000 _H - F83F FFFF _H	–	Reserved	SRIBE	SRIBE
F840 0000 _H - F840 FFFF _H	64 Kbyte	External Bus Unit (EBU0)	Access	Access
F841 0000 _H - F84F FFFF _H	–	Reserved	SRIBE	SRIBE
F850 0000 _H - F850 FFFF _H	64 Kbyte	DAM (DAM0)	Access	Access
F851 0000 _H - F851 FFFF _H	64 Kbyte	DAM (DAM1)	Access	Access
F852 0000 _H - F86F FFFF _H	–	Reserved	SRIBE	SRIBE
F870 0000 _H - F870 FFFF _H	64 Kbyte	SRI Domain 0 SFR (SRI0)	Access	Access
F871 0000 _H - F87F FFFF _H	–	Reserved	SRIBE	SRIBE
F880 0000 _H - F880 FFFF _H	64 Kbyte	CPU0 SFR (CPU0)	Access	Access
F881 0000 _H - F881 FFFF _H	64 Kbyte	CPU0 CSFR (CPU0)	Access	Access
F882 0000 _H - F882 FFFF _H	64 Kbyte	CPU1 SFR (CPU1)	Access	Access
F883 0000 _H - F883 FFFF _H	64 Kbyte	CPU1 CSFR (CPU1)	Access	Access
F884 0000 _H - F884 FFFF _H	64 Kbyte	CPU2 SFR (CPU2)	Access	Access
F885 0000 _H - F885 FFFF _H	64 Kbyte	CPU2 CSFR (CPU2)	Access	Access
F886 0000 _H - F886 FFFF _H	64 Kbyte	CPU3 SFR (CPU3)	Access	Access
F887 0000 _H - F887 FFFF _H	64 Kbyte	CPU3 CSFR (CPU3)	Access	Access
F888 0000 _H - F888 FFFF _H	64 Kbyte	CPU4 SFR (CPU4)	Access	Access

Memory Maps (MEMMAP)

Table 21 Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
F889 0000 _H - F889 FFFF _H	64 Kbyte	CPU4 CSFR (CPU4)	Access	Access
F88A 0000 _H - F88B FFFF _H	–	Reserved	SRIBE	SRIBE
F88C 0000 _H - F88C FFFF _H	64 Kbyte	CPU5 SFR (CPU5)	Access	Access
F88D 0000 _H - F88D FFFF _H	64 Kbyte	CPU5 CSFR (CPU5)	Access	Access
F88E 0000 _H - F88E FFFF _H	64 Kbyte	SRI Domain 1 SFR (SRI1)	Access	Access
F88F 0000 _H - F9FF FFFF _H	–	Reserved	SRIBE	SRIBE
FA00 0000 _H - FA00 00FF _H	–	Reserved	BBBBE	BBBBE
FA00 0100 _H - FA00 01FF _H	256 Byte	BBB Bus Control Unit (EBCU)	Access	Access
FA00 0200 _H - FA00 0FFF _H	–	Reserved	BBBBE	BBBBE
FA00 1000 _H - FA00 10FF _H	256 Byte	AGBT	Access	Access
FA00 1100 _H - FA00 5EFF _H	–	Reserved	BBBBE	BBBBE
FA00 6000 _H - FA00 60FF _H	256 Byte	EMEM Control Registers	Access	Access
FA00 6100 _H - FA00 FFFF _H	–	Reserved	BBBBE	BBBBE
FA01 0000 _H - FA01 FFFF _H	64 Kbyte	MCDS	Access	Access
FA02 0000 _H - FA03 FFFF _H	–	Reserved	BBBBE	BBBBE
FA04 0000 _H - FA04 01FF _H	512 Byte	Radar Interface 0 SFR (RIF0)	Access	Access
FA04 0200 _H - FA04 03FF _H	512 Byte	Radar Interface 1 SFR (RIF1)	Access	Access
FA04 0400 _H - FA6F FFFF _H	–	Reserved	BBBBE	BBBBE
FA70 0000 _H - FA70 00FF _H	256 Byte	SPU Lockstep SFR	Access	Access
FA70 0100 _H - FA7F FFFF _H	–	Reserved	BBBBE	BBBBE
FA80 0000 _H - FA80 07FF _H	2 Kbyte	Signal Processing Unit 0 SFR (SPU0)	Access	Access
FA80 0800 _H - FA9F FFFF _H	–	Reserved	BBBBE	BBBBE
FAA0 0000 _H - FAA0 FFFF _H	64 Kbyte	SPU0 Configuration RAM (SPUCFG0)	Access	Access
FAA1 0000 _H - FABF FFFF _H	–	Reserved	BBBBE	BBBBE
FAC0 0000 _H - FAC0 07FF _H	2 Kbyte	Signal Processing Unit 1 SFR (SPU1)	Access	Access
FAC0 0800 _H - FADF FFFF _H	–	Reserved	BBBBE	BBBBE
FAE0 0000 _H - FAE0 FFFF _H	64 Kbyte	SPU1 Configuration RAM (SPUCFG1)	Access	Access
FAE1 0000 _H - FAFF FFFF _H	–	Reserved	BBBBE	BBBBE
FB00 0000 _H - FB00 FFFF _H	64 Kbyte	EMEM SRI Slave Interface 0 SFR	Access	Access
FB01 0000 _H - FB01 FFFF _H	64 Kbyte	EMEM SRI Slave Interface 1 SFR	Access	Access
FB02 0000 _H - FB02 FFFF _H	64 Kbyte	EMEM SRI Slave Interface 2 SFR	Access	Access
FB03 0000 _H - FB03 FFFF _H	64 Kbyte	EMEM SRI Slave Interface 3 SFR	Access	Access
FB04 0000 _H - FB6F FFFF _H	–	Reserved	SRIBE	SRIBE
FB70 0000 _H - FB70 FFFF _H	64 Kbyte	SRI Domain 2 SFR (SRI2)	Access	Access
FB71 0000 _H - FB71 7FFF _H	32 Kbyte	Reserved	SRIBE	SRIBE
FB71 8000 _H - FB71 FFFF _H	32 Kbyte	MINIMCDS SFR (MINIMCDS)	Access ²⁾	Access ²⁾
FB72 0000 _H - FBFF FFFF _H	–	Reserved	SRIBE	SRIBE

Memory Maps (MEMMAP)

Table 21 Address Map of Segment 15 (cont'd)

Address Range	Size	Unit	Access Type	
			Read	Write
FC00 0000 _H - FFBF FFFF _H	–	Reserved	SRIBE	SRIBE
FFC0 0000 _H - FFC1 FFFF _H	128 Kbyte	Data Flash 1 EEPROM (DF1) HSM Command Sequence Interpreter	Access	Access ³⁾
FFC2 0000 _H - FFC3 FFFF _H	128 Kbyte	Reserved	SRIBE	SRIBE
FFC4 0000 _H - FFFF FFFF _H	–	Reserved	SRIBE	SRIBE

1) TC38x only

2) MINIMCDS SFR may only be accessed when OCDS is enabled.

3) HSM Command Sequence Interpreter